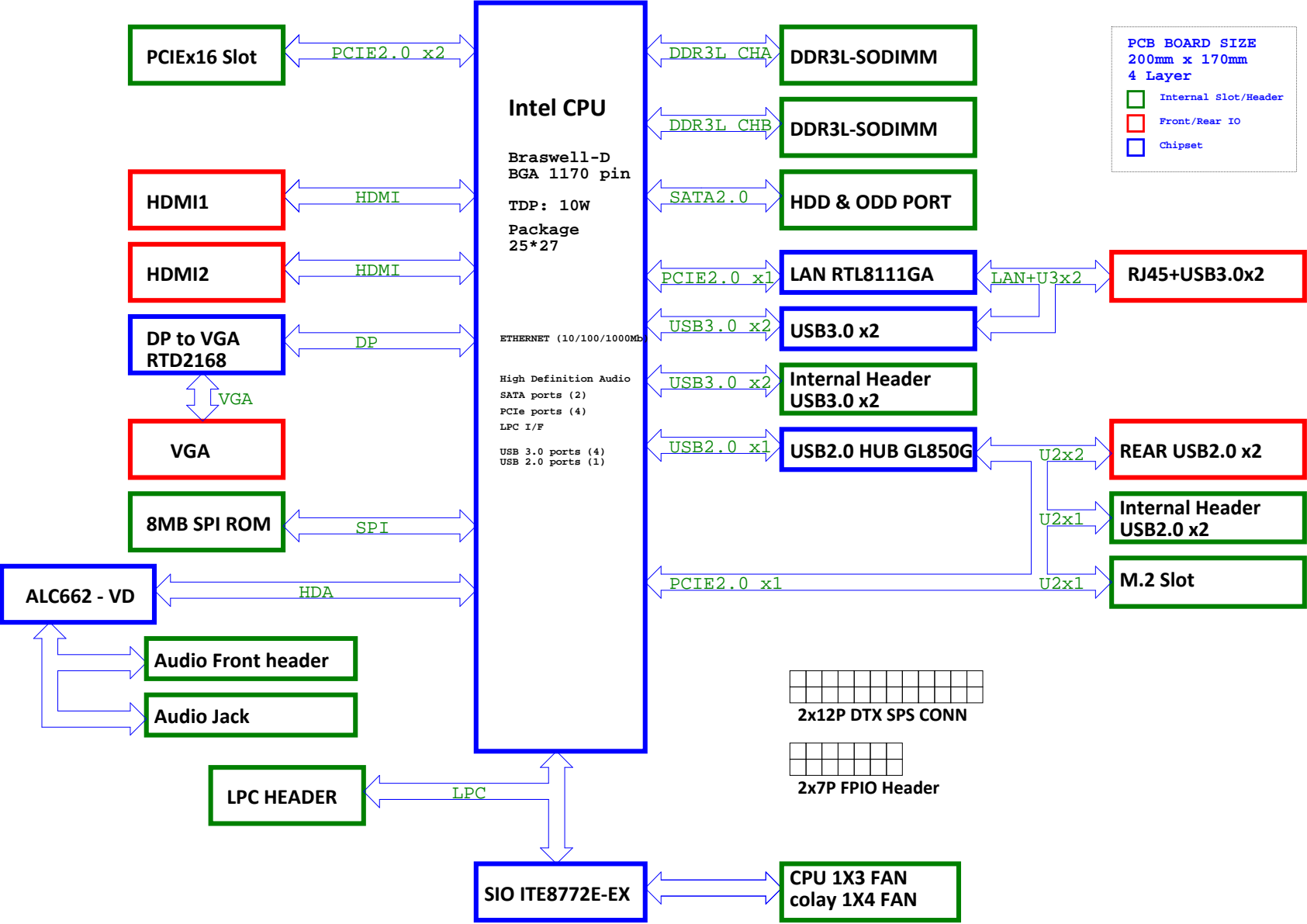






Project Name: Brian  
Project Code: 91.N0000.021  
PCB Number : 14074-SA



(Reserved)

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Title <b>CPU (DMI/FDI) (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 3 of 108	

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>CPU (THERMAL/CLK) (Reserved</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 4 of 108	



(Reserved)



**Wistron Incorporated**  
21F, 88, Sec.1,Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title  
**CPU (CFG) (Reserved)**

Size A	Document Number <b>Braswell</b>	Rev SA
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Date:	Tuesday, March 24, 2015	Sheet	6	of	111
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# Braswell-M/D Platform Display Configuration

	Default	1	2	3	4	5	6	7
DDI-0	DP	DP	DP	DP	HDMI	HDMI	HDMI	HDMI
DDI-1	eDP	eDP	DP	HDMI (4-lane)	eDP	eDP	DP	HDMI (4-lane)
DDI-2	HDMI	DP	HDMI	HDMI	HDMI	DP	HDMI	HDMI
PCU UART	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No

Table 139. DDI Disable Guidelines

Signal	Recommendation
DDIx_TXP[3:0]	NC
DDIx_TXN[3:0]	NC
DDIx_AUXP	NC
DDIx_AUXN	NC
DDIx_HPD	GND
DDIx_DDCCLK	GND
DDIx_DDCDATA	NC
DDIx_VDDEN	NC
DDIx_BKLTEN	NC
DDIx_BKLTCL	NC
DDIx_RCOMP	NC

## 10.8 Unused Interface Termination

Table 53. MIPI+CSI-2 Pins

Signal Name	Action
NCSL[3:1]_CLKP	No connect
NCSL[3:1]_CLKN	No connect
NCSL[3:1]_DP[0:3]	No connect
NCSL[3:1]_DP[0:3]	No connect
NCSL[3:1]_DP[0:3]	No connect
NCSL[3:1]_DP[0:3]	No connect
NCSL[3:1]_DP[0:3]	No connect
NCSL[3:1]_DP[0:3]	No connect

NOTE: If a x1 or x2 or x3 Camera is used on MCSL\_X4 port, closing some lines to be disconnected, these unused signals can be no connect.

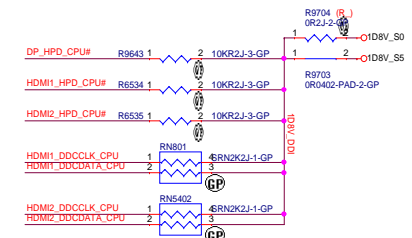
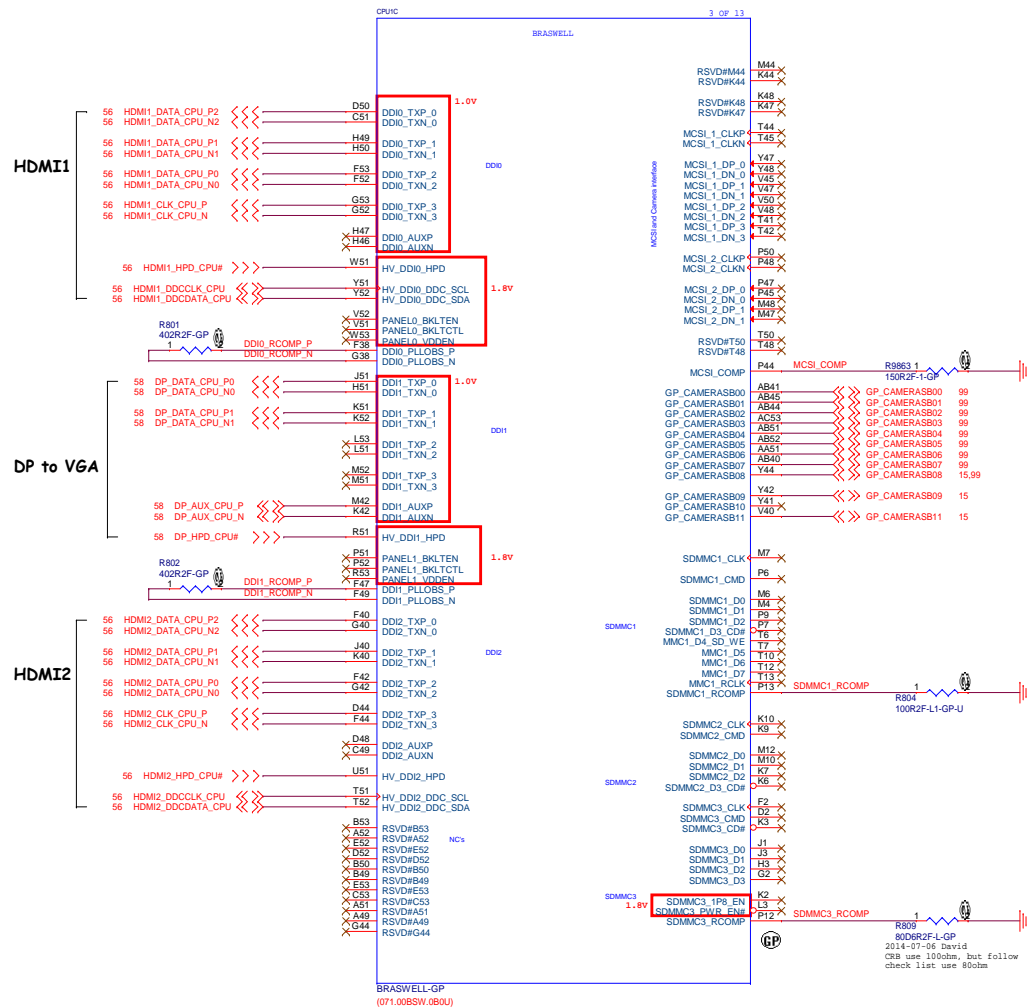
## 20.2.2 SD Card Disable Guidelines

Each signal may left as a No Connect or used as a GPIO. Additional consideration for each option are listed below.

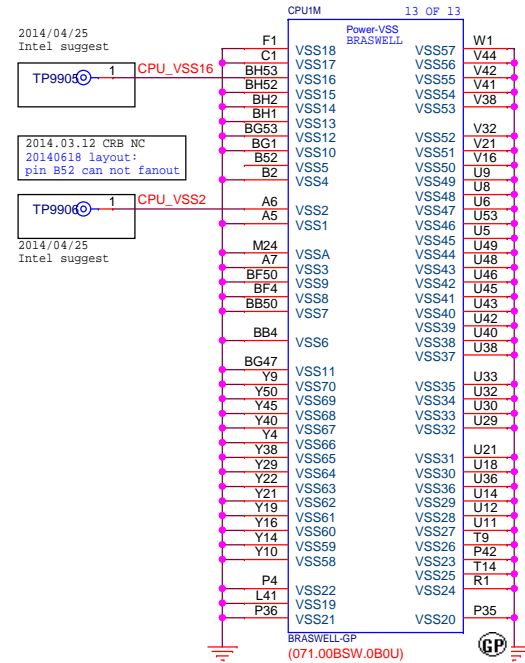
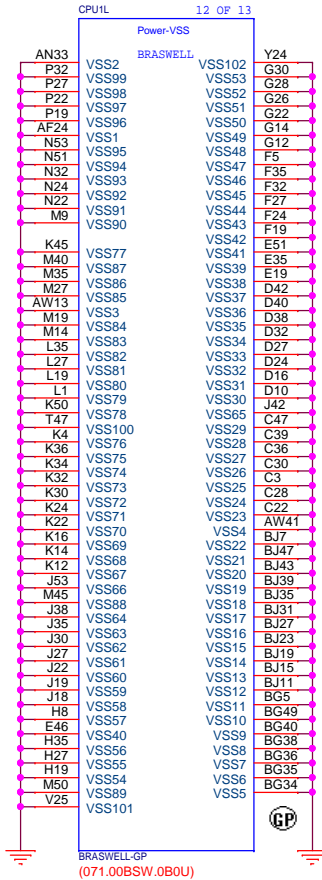
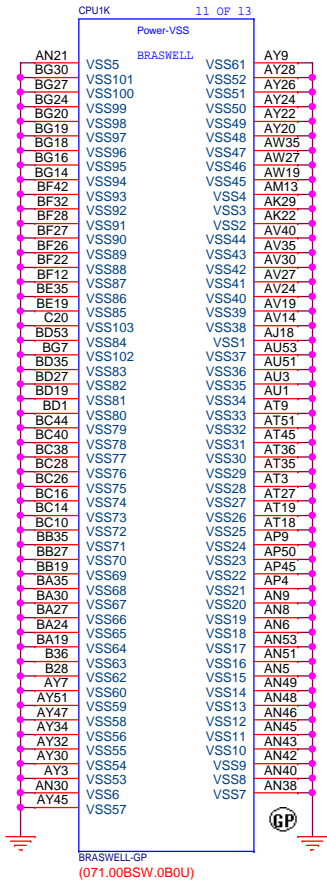
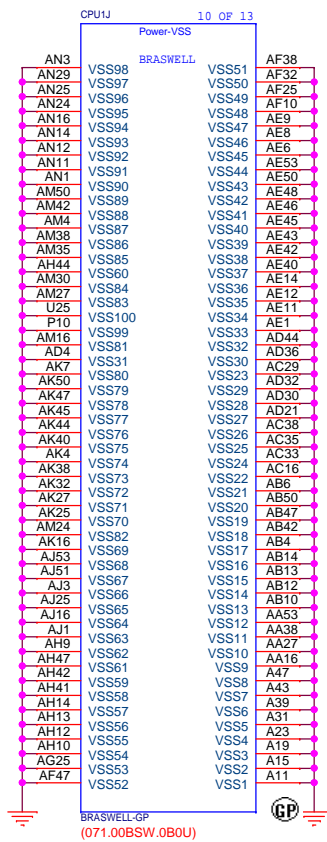
**No Connect** – Disable the relevant interface controller via the corresponding Soft Strap listed in the SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPIO via system BIOS. See the BIOS Writers Guide for further details.

**GPIO** – Disable the relevant interface controller via the corresponding Soft Strap listed in the SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPIO or GPIO via system BIOS. See the BIOS Writers Guide for further details.

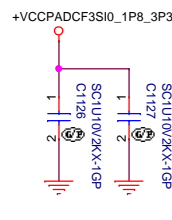
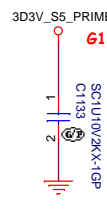
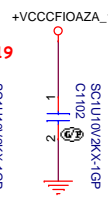
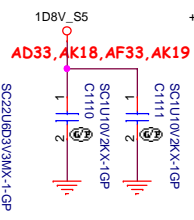
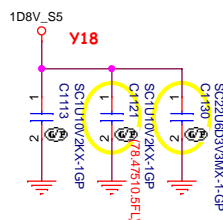
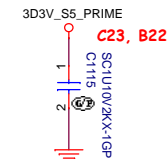
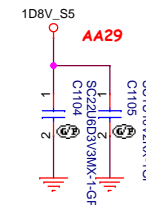
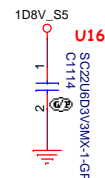
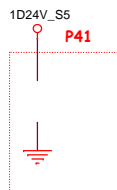
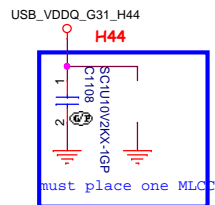
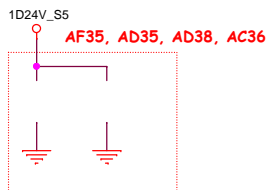
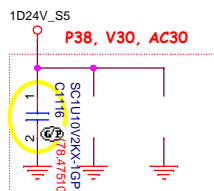
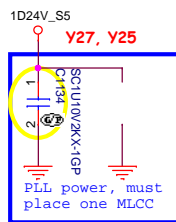
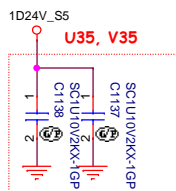
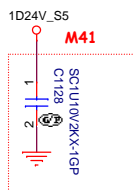
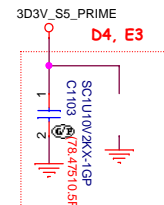
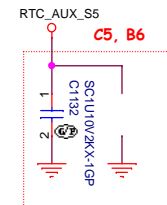
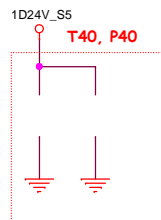
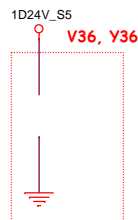
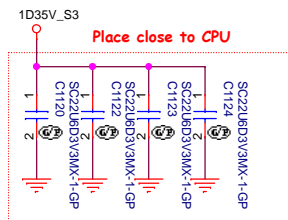
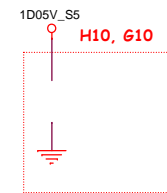
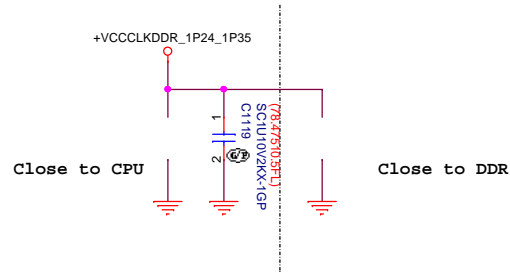
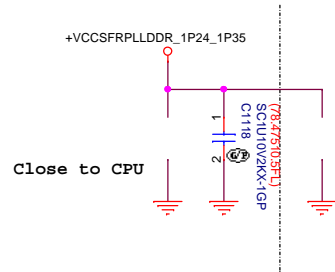
The RCOMP should always pull-down with 100 kΩ ±1%.













20140706  
follow CRB

SPD SA1	0
SPD SA0	1

**DIMM1 Reset**

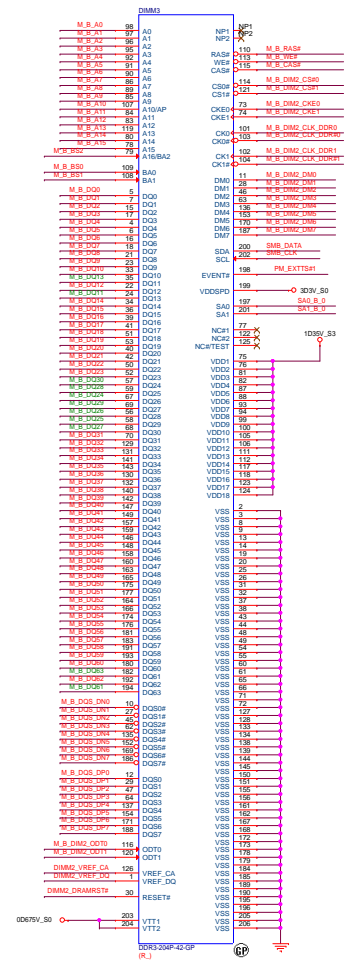
5 M\_B\_DRAMRST# 2 1 DIMM2\_DRAMRST#

R1216


GR0402-PAD-2-0P

C1227 SC18P50V2K1X-15P

C1228 SC18P50V2K1X-15P



(Reserved)

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Title <b>SODIMM3_SODIMM4 (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 14 of 111	

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE K02 AREA1-2: Enable TXE  
2-3: Disable TXE  
Could be override

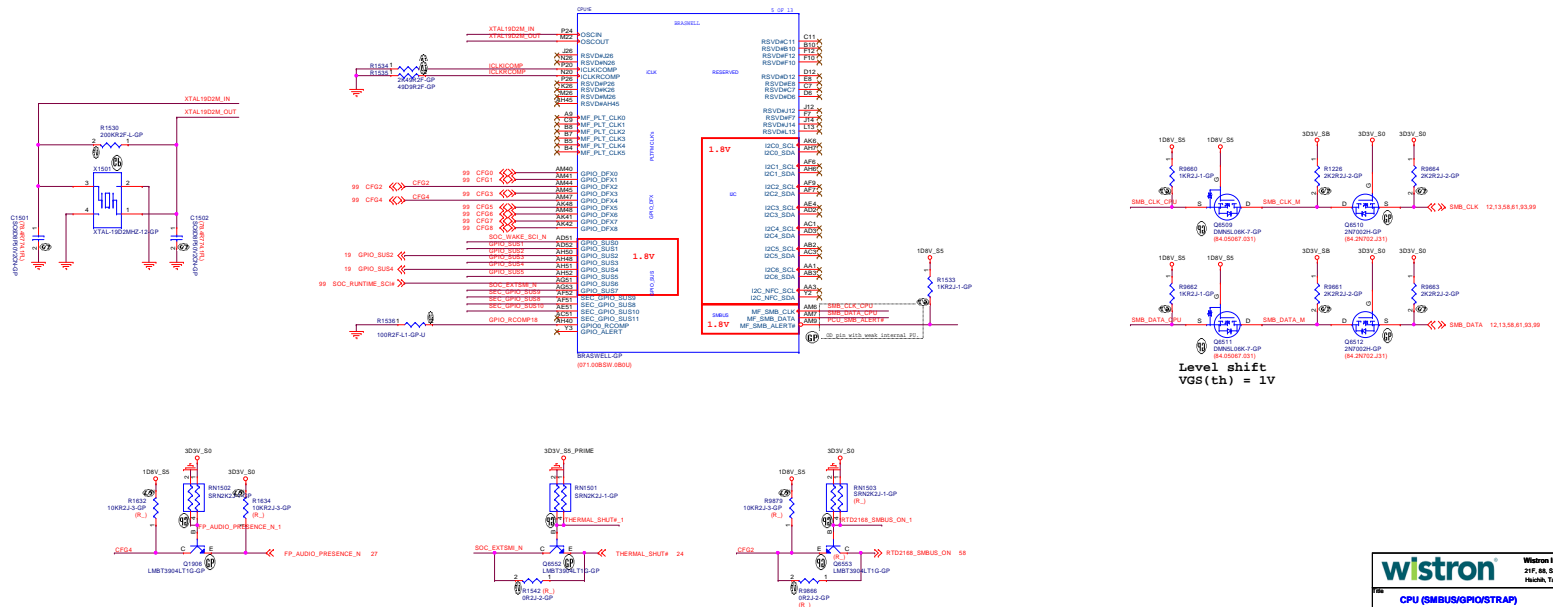
Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
<b>GPIO</b>	<b>GPIO_SUS0</b> (Weak Internal pull-down)	<b>GPIO_SUS1</b> (Weak Internal pull-down)	<b>GPIO_SUS2</b> (Weak Internal pull-up)	<b>GPIO_SUS3</b> (Weak Internal pull-down)	<b>GPIO_SUS4</b> (Weak Internal pull-up)	<b>GPIO_SUS5</b> (Weak Internal pull-up)	<b>GPIO_SUS6</b> (Weak Internal pull-up)	<b>GPIO_SUS7</b> (Weak Internal pull-up)	<b>SEC_GPIO_SUS8</b> (Weak Internal pull-up)	<b>SEC_GPIO_SUS9</b> (Weak Internal pull-down)	<b>SEC_GPIO_SUS10</b> (Weak Internal pull-down)	<b>GP_CAMERASB08</b> (Weak Internal pull-down)	<b>GP_CAMERASB09</b> (Weak Internal pull-down)	<b>GP_CAMERASB11</b> (Weak Internal pull-down)
<b>Schematic</b>														
<b>High</b>	<b>DDI0 Detect (V)</b>	<b>DDI1 Detect (V)</b>	<b>Normal Operation (V)</b>	<b>DSI Detect</b>	<b>Boot from SPI (V)</b>	<b>Normal Operation</b>	<b>Normal (V)</b> (Follow CBB)	<b>Normal (V)</b> (Follow CBB)	<b>1.35V</b>	<b>Bypass with 1.05V (V)</b>	<b>PMC</b>	<b>Bypass</b>	<b>Bypass</b>	<b>Bypass</b>
<b>Low</b>	<b>Not Detect</b>	<b>Not Detect</b>	<b>Change Boot Loader address(A16 Override)</b>	<b>Not Detect (V)</b> (Follow CBB)	<b>Boot from LPC</b>	<b>Override</b>	<b>Halt boot enable</b>	<b>Sus Debug enable</b>	<b>1.25V (V)</b>	<b>No bypass</b> <small>SPEC not match with CBB</small>	<b>Fuse controller (V)</b> <small>Check Function</small>	<b>No Bypass (V)</b>	<b>No Bypass (V)</b>	<b>No Bypass (V)</b>

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = SPI 1 = Normal Operation
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

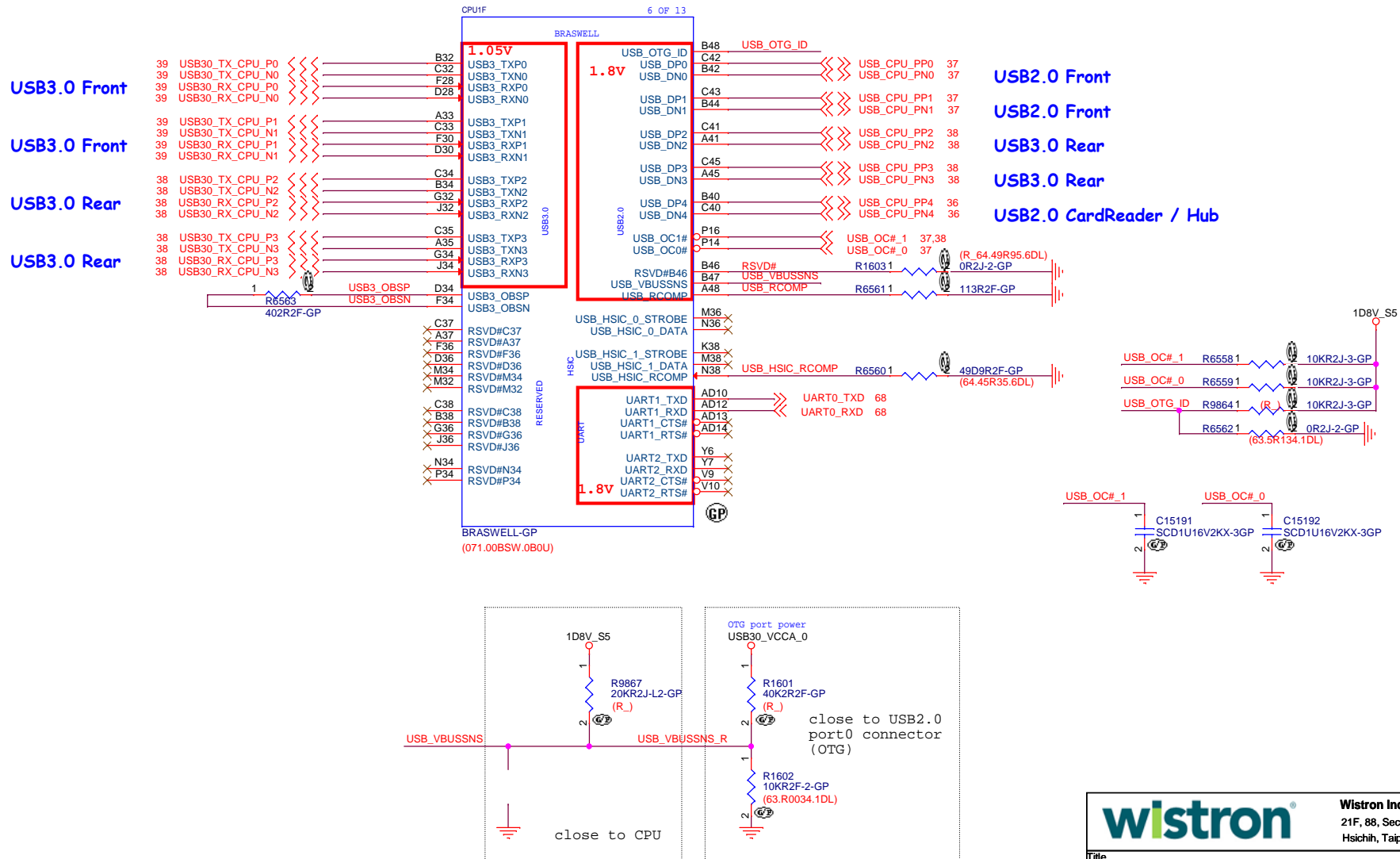
Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V  This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass




20140717 David  
SA節省修改時間，直接換port  
SB要把port number改為對應的數字

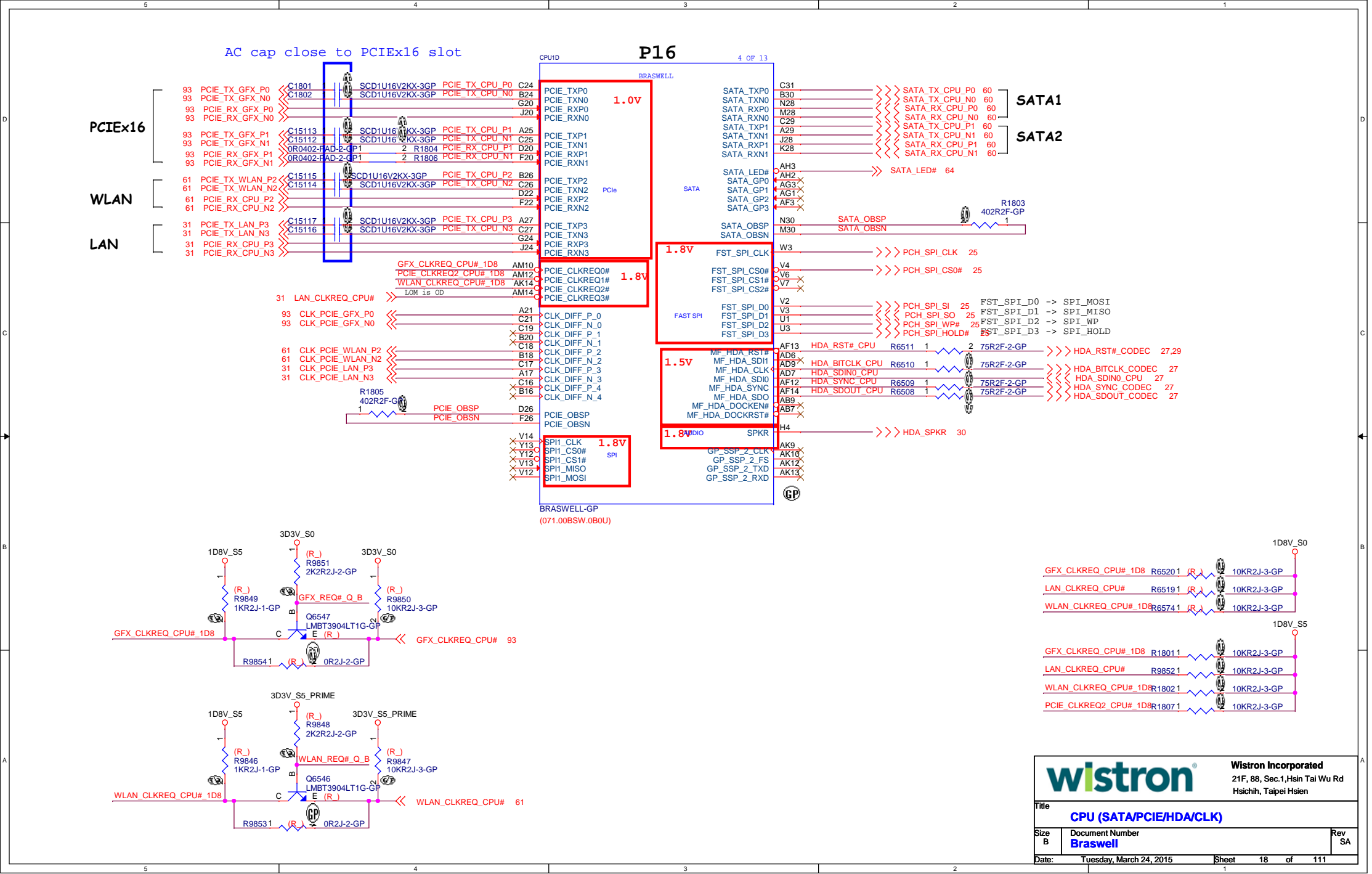
20140905 Gary  
修改為正常的port number






(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>CPU (DMI/FDI) (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 17 of 111	

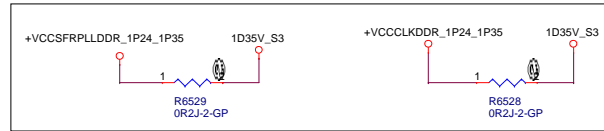




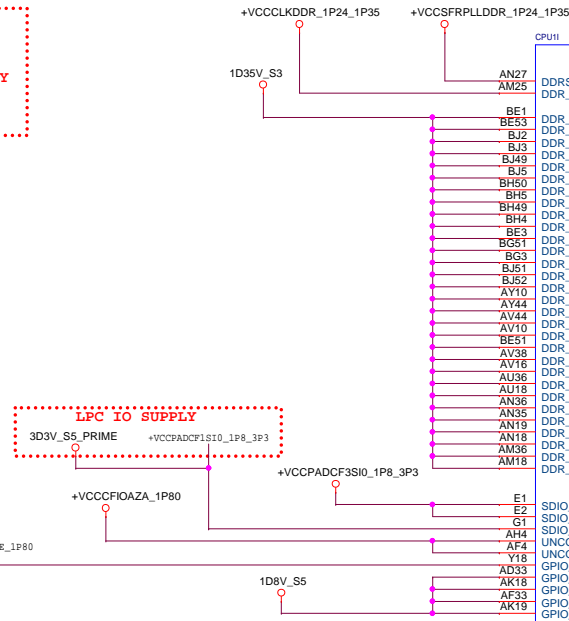
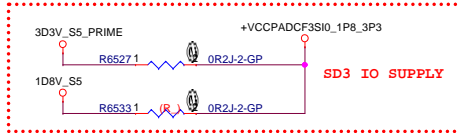
(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>CPU (GPIO/CPU) (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	20 of 111

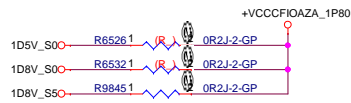
2014.03.21 change page



redwood connect to 3.3V\_S0, check with Intel




AUDIO IO SUPPLY




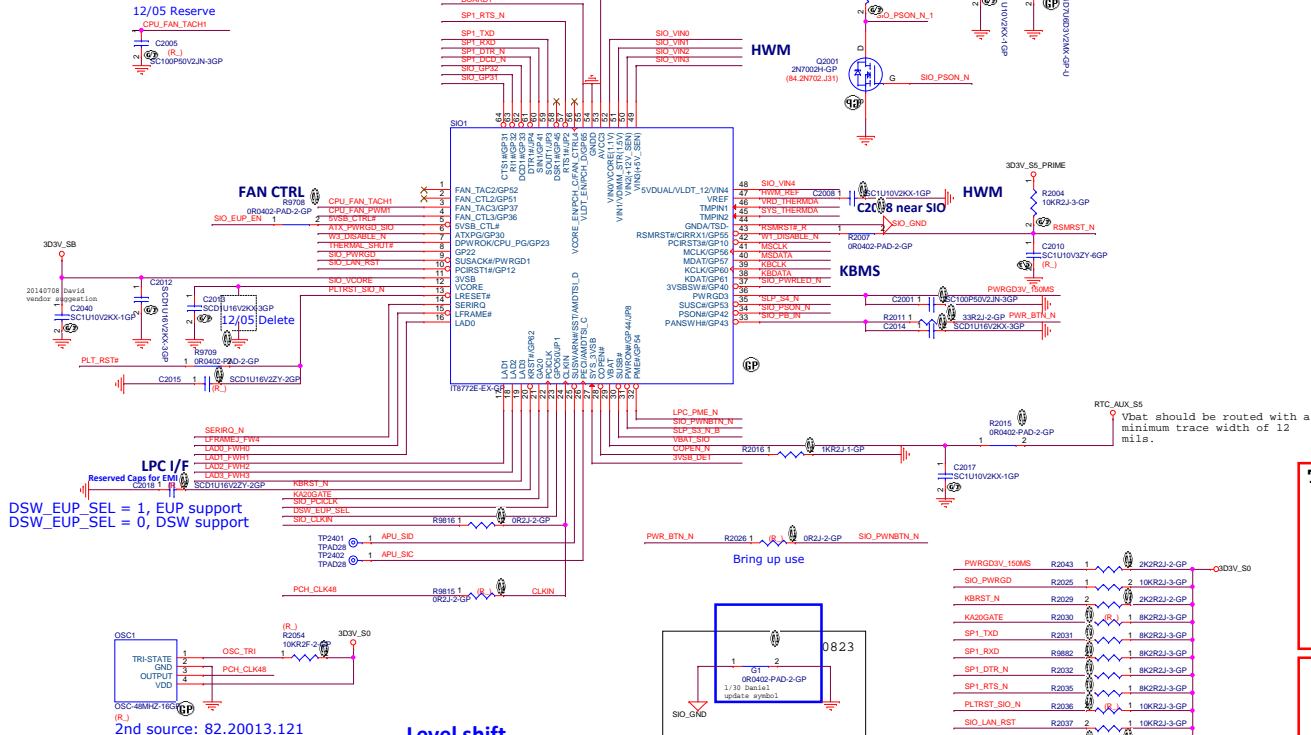
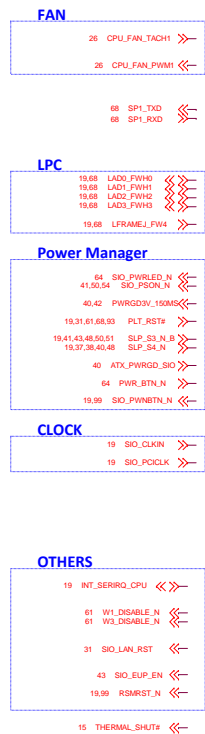
2015/12/21 David  
change to 1D8V\_S5 to save 1D5V LDO

(Reserved)

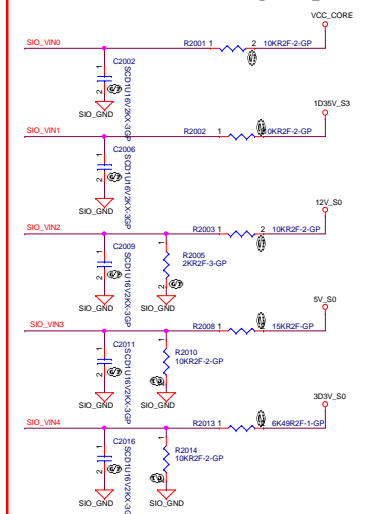
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>CPU (POWER2) (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	22 of 111

(Reserved)

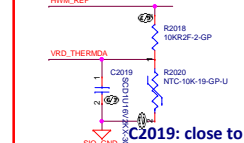
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>CPU (VSS) (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	23 of 111



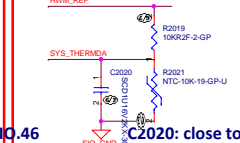
## SIO PWR monitoring inputs



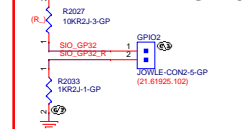
## Thermistor (VRD) Place Close to VRD



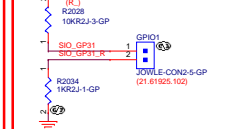
## Thermistor (SYS) Place Close to SIO



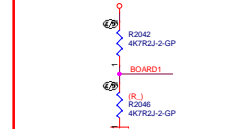
## GPIO



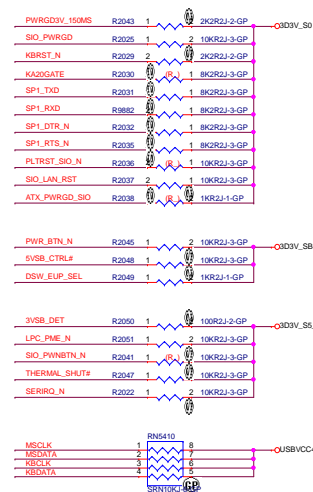
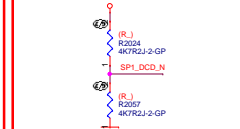
## GPIO



## Board ID

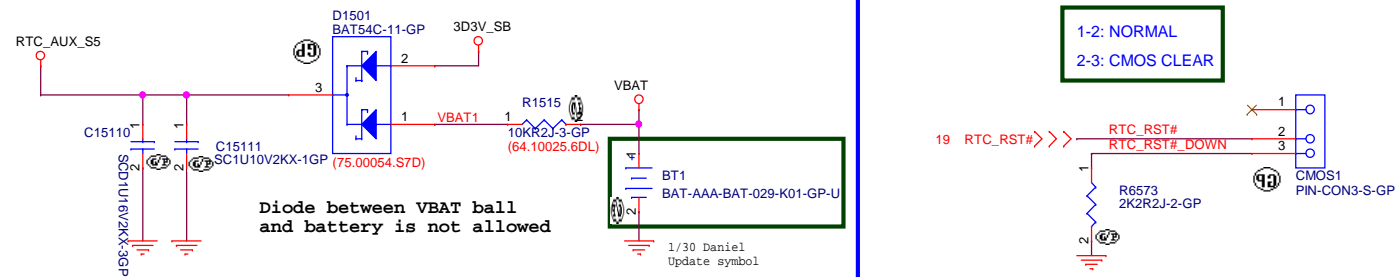
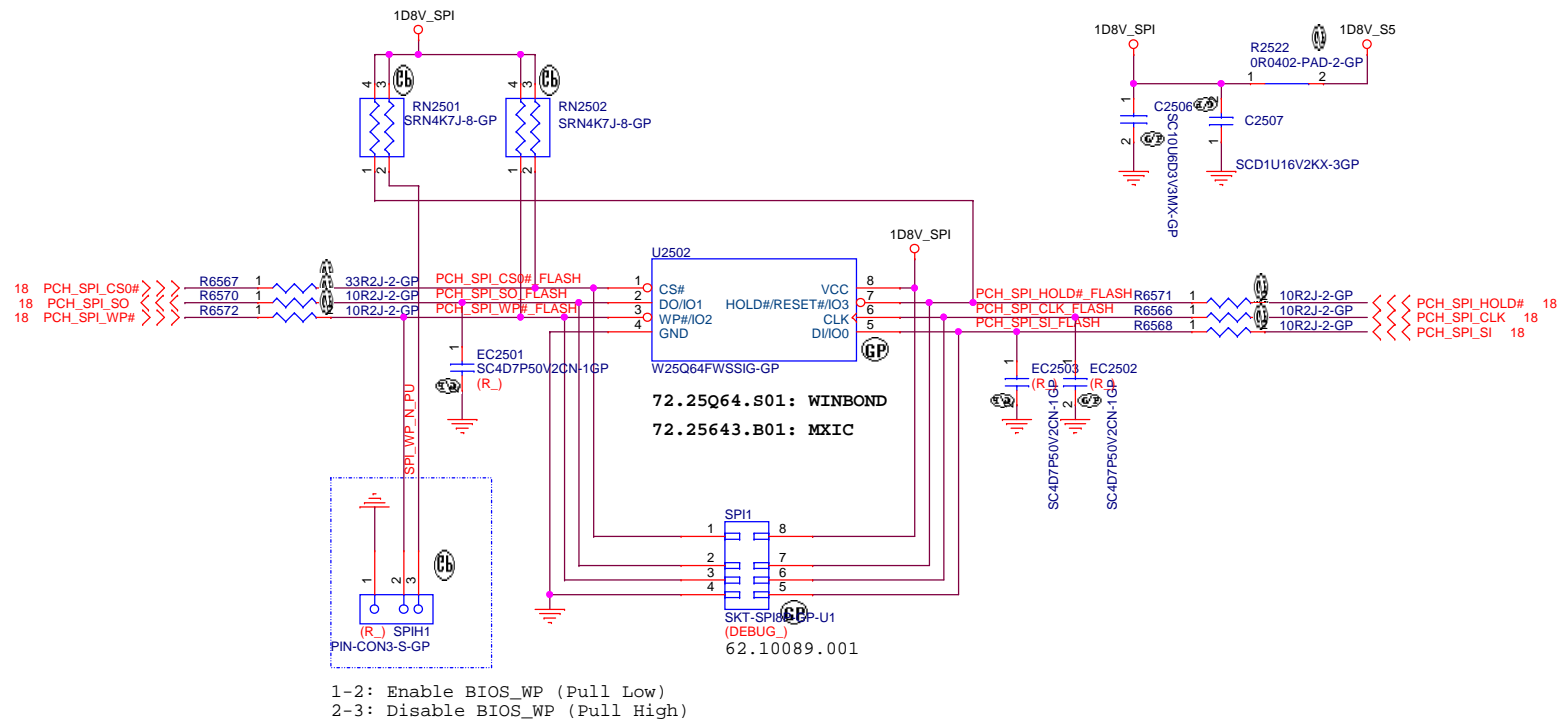


## Board ID





## SPI FLASH ROM (8M Byte) for PCH



```
24 CPU_FAN_TACH1
24 CPU_FAN_PWM1
```

```
20140703 David
Remove SYS FAN for layout space
```

**CPU FAN**  
**SYS 3 PINS/4 PINS FAN CONTROL**


### Option for 3PIN CTRL

### Co-layout with FANCD2

Bogis 20131001  
Un-mount R2509  
Mount R2501 R2508 R2511 R2512 R2514 R2515 R2516  
Mount C2503 TC2501 Q2501 Q2502 Q2503



(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>AMP (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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27 FP\_OUTR\_LL <<=====

27 FP\_OUTR\_RR <<=====

27 MIC2\_LL <<=====

27 MIC2\_RR <<=====

27 AUD\_IN\_L >>=====

27 AUD\_IN\_R >>=====



Change 10U MLCC  
03/17

Removed 22k resistor  
04/06



```

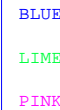
27 LINEIN_JD  <<-----
27 FRONT_JD   <<-----
27 MIC1_JD    <<-----

```



INCREASE VREF CAP IF  
POP IS PRESENT

AGND



NOTE:  
MIC GROUND ROUT BACK TO CODEC  
ALONG WITH MIC\_TRACE.  
TIE MIC\_GND TO AGND NEAR CODEC

CODEC Removed 22k resist  
04/06

NOTE:  
MIC GROUND ROUT BACK TO CODEC  
ALONG WITH MIC\_TRACE.  
TIE MIC\_GND TO AGND NEAR CODEC

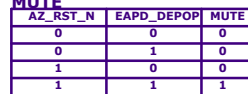
Control by software driver and CODEC GPIO.  
GPIO driving low at:

- 1).Initial state
- 2).Suspend to S1
- 3).Resume from S1.

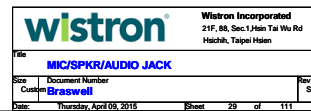


Unmount R2725, Mount R2726

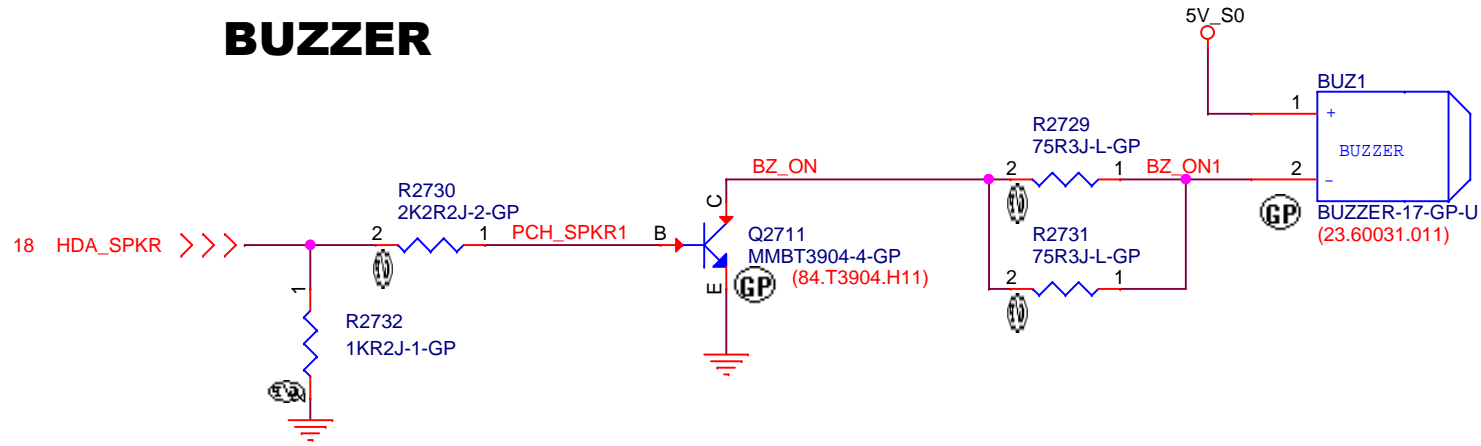
Add & reserve 0.1uF for pop-noise  
05/05



AZ_RST_N	EAPD_DEPOP	MUTE
0	0	0
0	1	0
1	0	0
1	1	1



# BUZZER



**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title

**AUDIO JACK/BUZZER**

Size  
A

Document Number  
**Braswell**

Rev  
SA

Date: Tuesday, March 24, 2015

Sheet 30 of 111

32 LAN\_LINK\_1000  
32 LAN\_LINK\_100  
LAN\_LED\_ACTIVE

18 PCIE\_TX\_LAN\_P3  
18 PCIE\_TX\_LAN\_N3  
18 PCIE\_RX\_CPU\_P3  
18 PCIE\_RX\_CPU\_N3

18 CLK\_PCIE\_LAN\_P3  
18 CLK\_PCIE\_LAN\_N3

32 LAN\_MDIO\_DP  
32 LAN\_MDIO\_DN

32 LAN\_MDI1\_DP  
32 LAN\_MDI1\_DN

32 LAN\_MD2\_DP  
32 LAN\_MD2\_DN

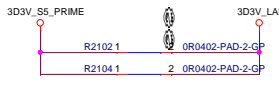
32 LAN\_MD3\_DP  
32 LAN\_MD3\_DN

24 SIO\_LAN\_RST

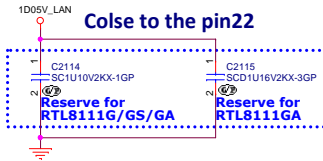
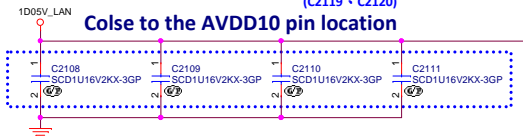
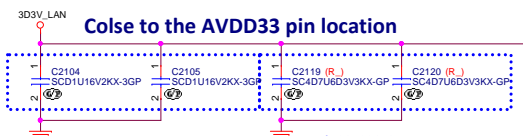
9,24,61,68,93 PLT\_RST#

19 PCIE\_WAKE\_LOM

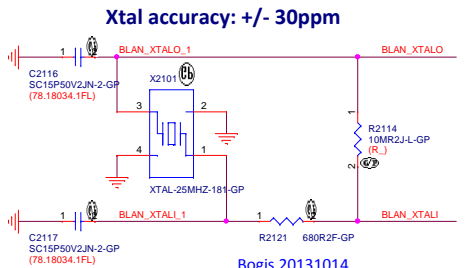
18 LAN\_CLKREQ\_CPU#



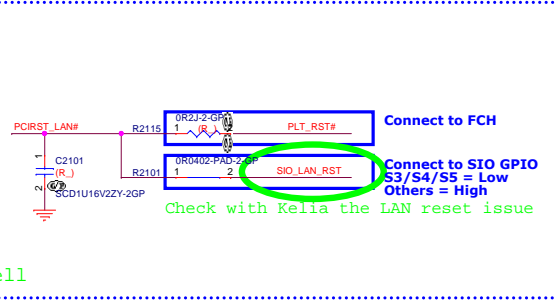
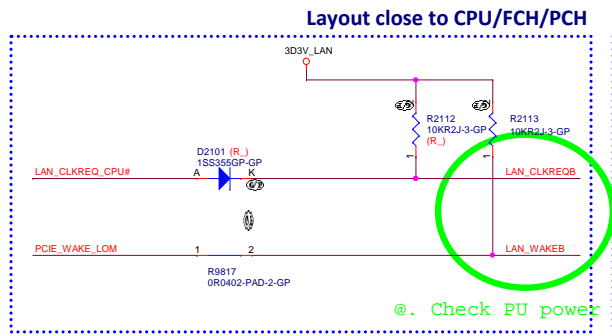
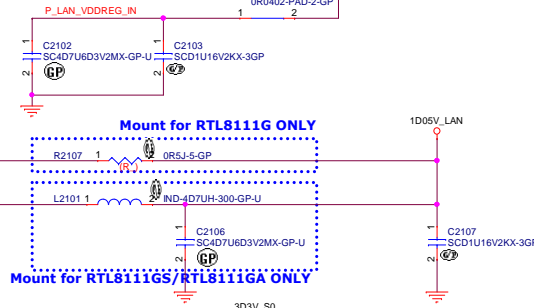
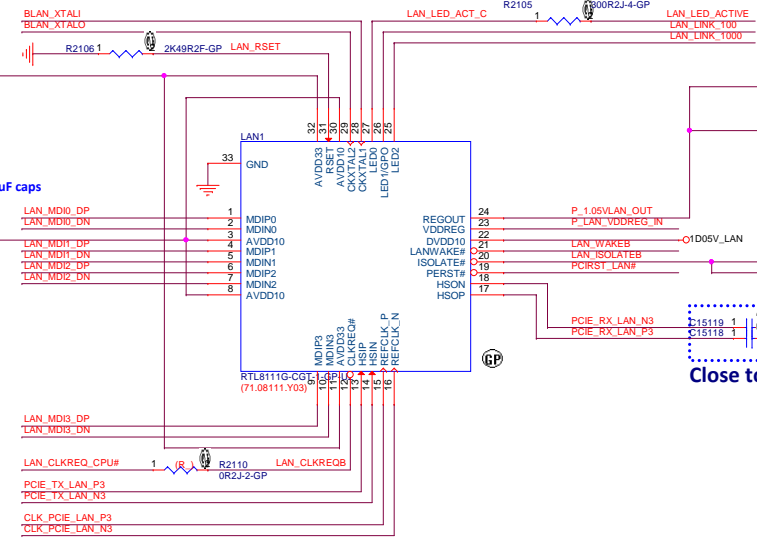
+3VM\_LAN rise time:  
0.5mS ~ 100mS.



Bogis 20130723  
Connect R1934.2 from +1P8V\_DUAL to 1D8V\_S0  
Del R1936 R1935 Q1904  
Short PCIE\_CLK\_LAN\_REQ#\_CPU to PCIE\_CLK\_LAN\_REQ#  
Unmount R1934

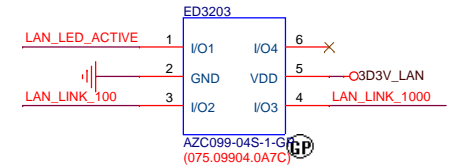
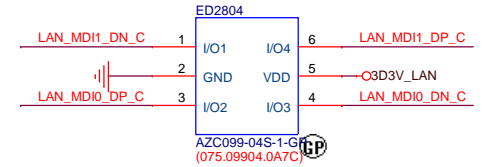
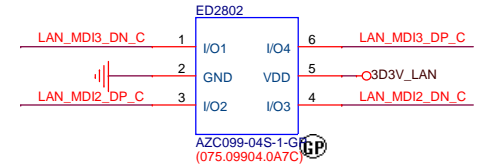
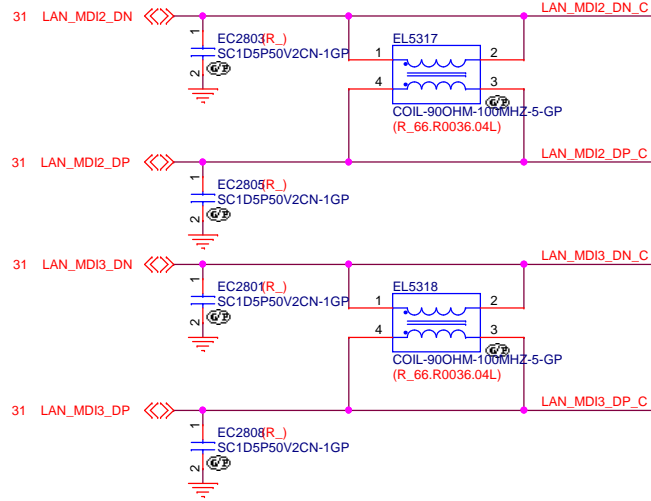
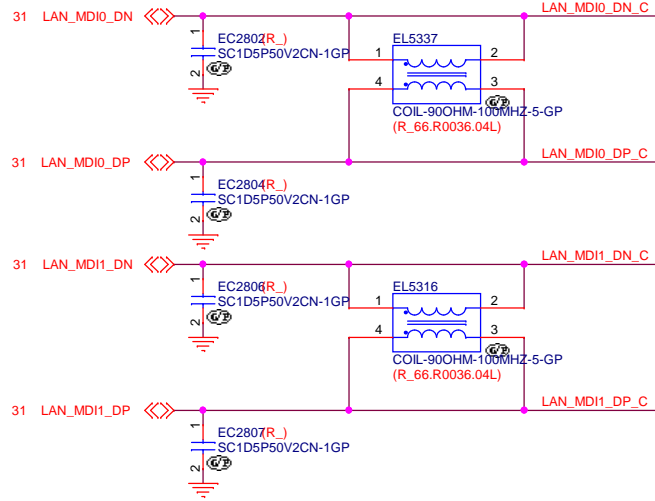


Bogis 20131014  
Add R2121 by vendor test result

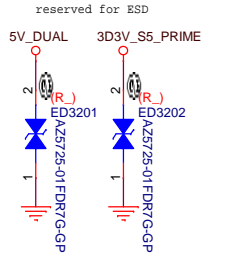
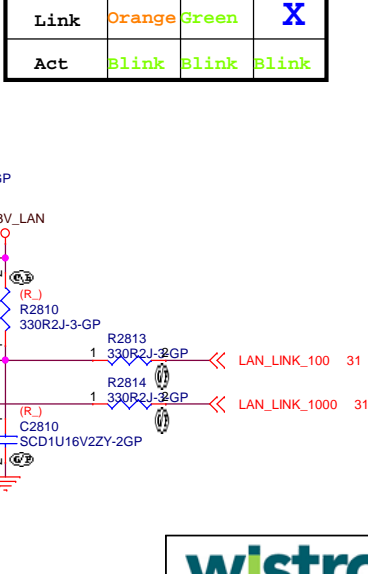
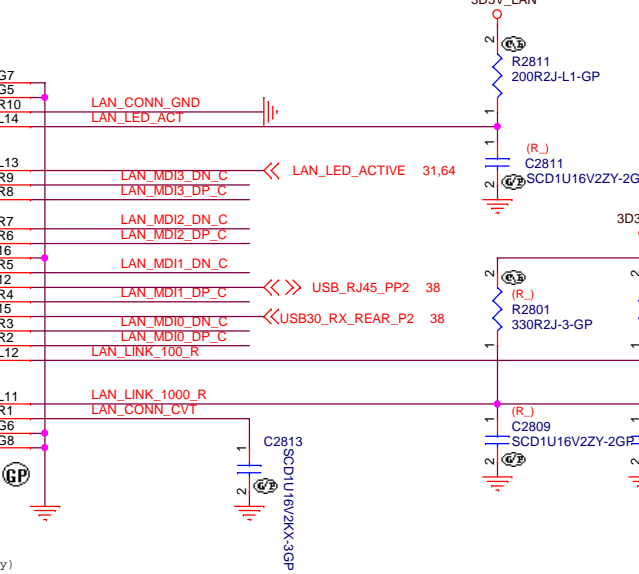
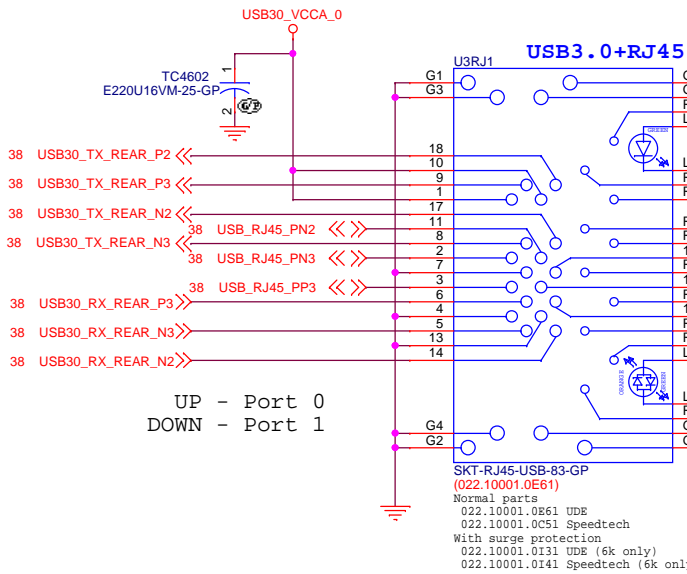


Bogis 20130717  
Del Q2101, add D2101  
Unmount R2112 D2101

# LAN common choke




	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink






	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	


(Reserved)

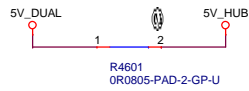
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Card Reader IC/Slot</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 33 of 111	

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>USB Charger (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	34 of 111

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>USB redriver (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	35 of 111



## GL850G

Enable/Disable USB output port: D+/D- pull high 1K to disable USB port

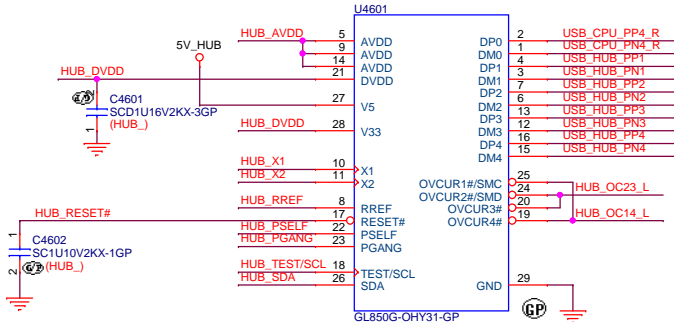
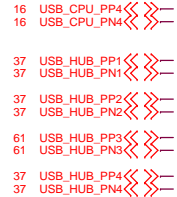
Set USB port to be internal (non-removable): set OC pin is floating

Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

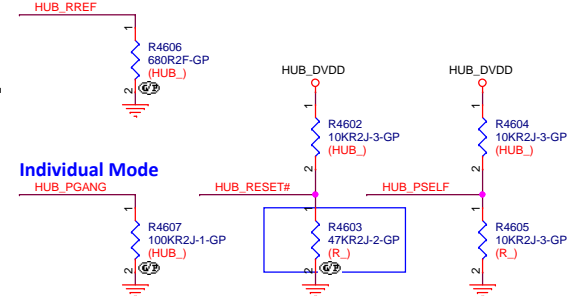
## GL852G

Enable/Disable USB output port: setting by EEPROM

Set USB port to be internal (non-removable) or external (removable): setting by EEPROM



From SoC  
To Rear USB2.0  
To FIO Card Reader  
To Mini PCIE for BT  
To Rear USB2.0



HUB\_PSELF = 1 if self-powered  
HUB\_PSELF = 0 if bus-powered

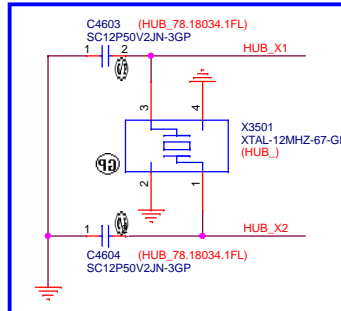
GL850G-OHY31-GP  
(HUB\_071.0850G.0003)

Co-lay GL850G and GL852G

GL850G: 71.0850G.003 (USB2.0 STT 1 to 4)

GL852G: 71.00852.A03 (USB2.0 MTT 1 to 4)

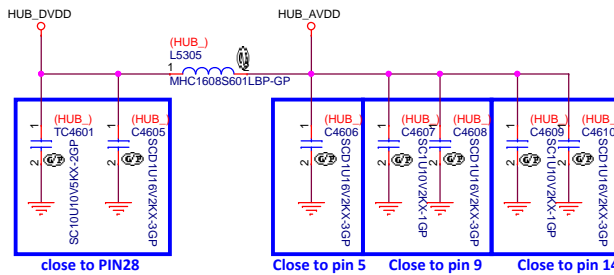
Xtal accuracy: +/- 30ppm



Close to GL850G pin10/11

## Internal Power

(Hub Internal VR output from pin 28 V33 = HUB\_DVDD)



close to PIN28

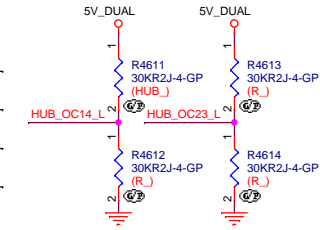
Close to pin 5

Close to pin 9

Close to pin 14

## Over Current

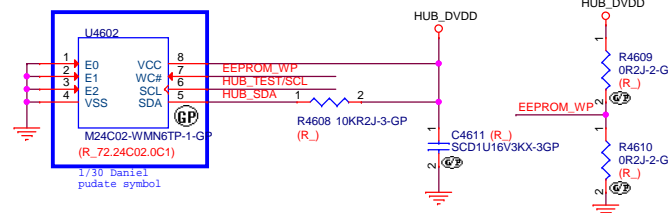
	R divider Removable	Floating Non-Removable
OVCUR1#	V	
OVCUR2#		V
OVCUR3#		V
OVCUR4#	V	
	external	internal



Bogis 20131014  
Change X3501 to 82.30006.641  
2nd source: 82.30006.501

## EEPROM

EEPROM is used for customized VID, PID, String, Configuration  
The purpose is to set 4 USB ports to be internal/external  
Default settings: 4 ports are external ports



## USB Table

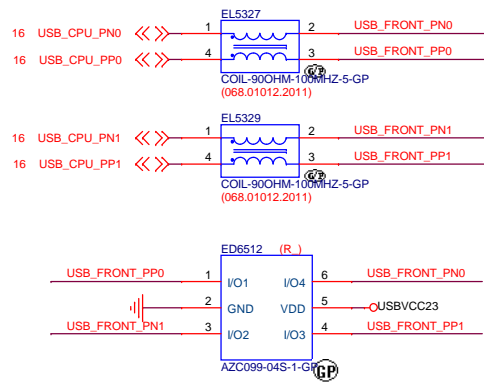
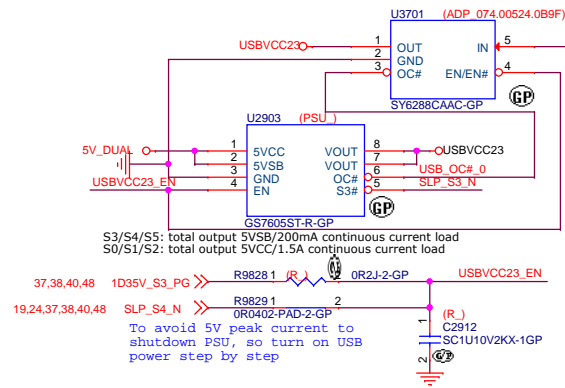
Pair	Device
1	Rear USB2.0 I/O port
2	Internal USB2.0 for Card reader
3	Internal USB2.0 for BT
4	Rear USB2.0 I/O port

external  
internal  
internal  
external

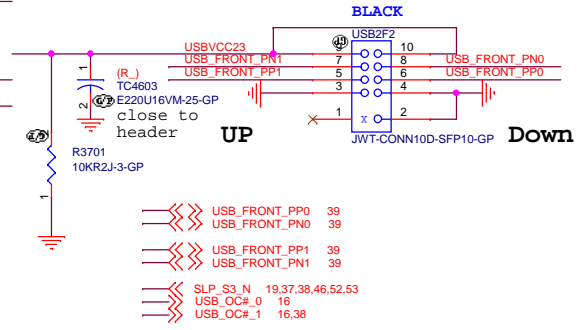
**wistron**

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21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

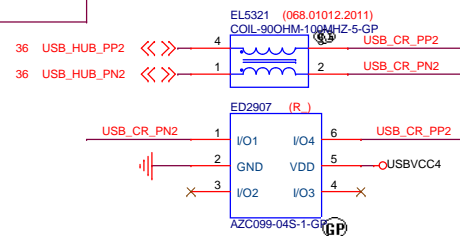
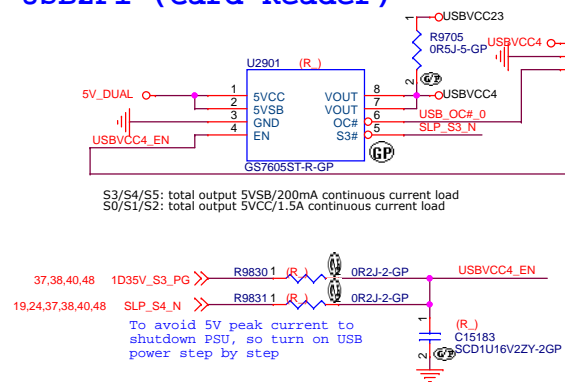
## For USB2F2 (Front USB2.0 x2)



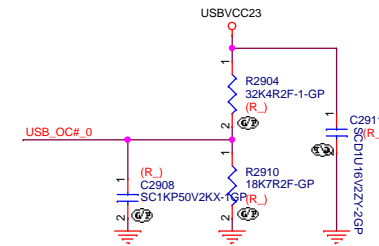
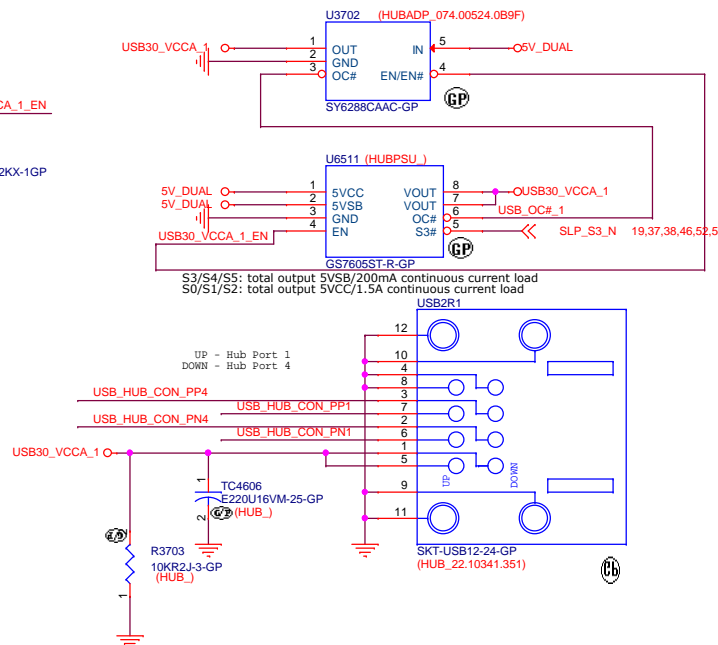
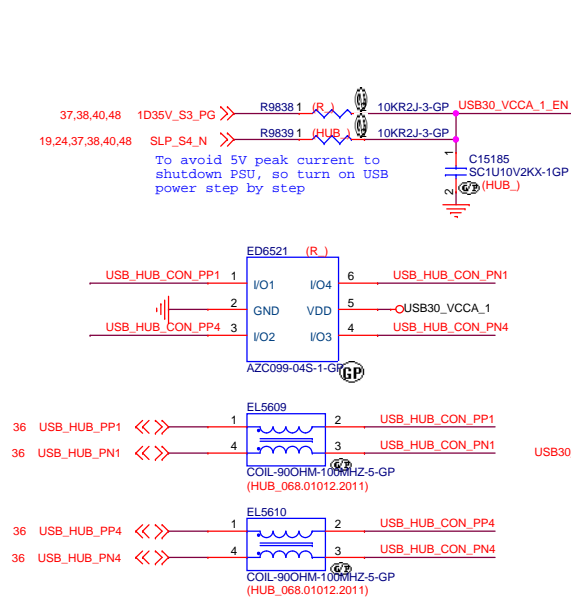
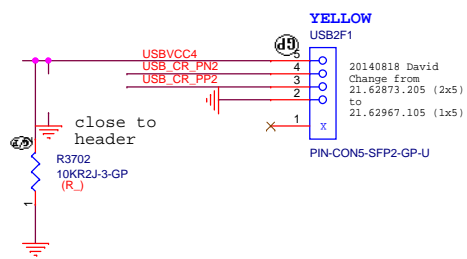
## FP Header USB2.0 Co-lay with front USB3.0



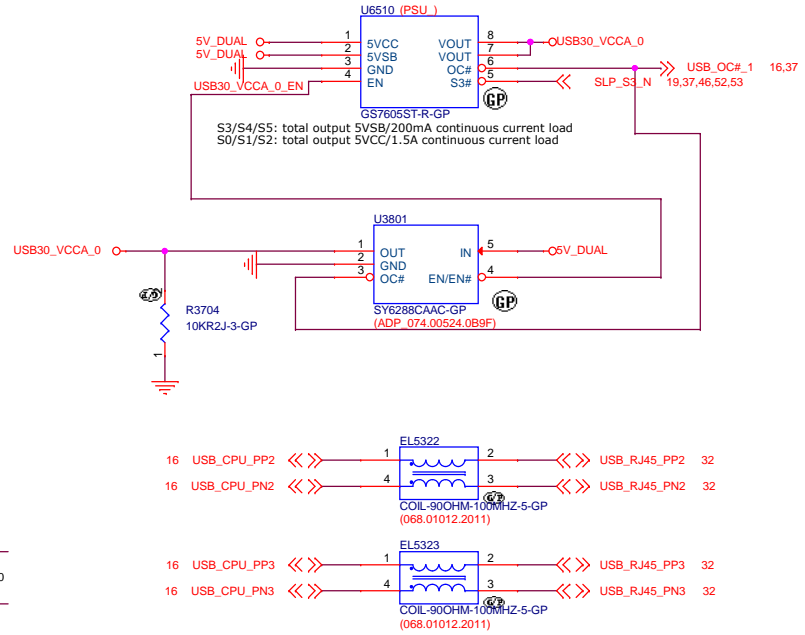
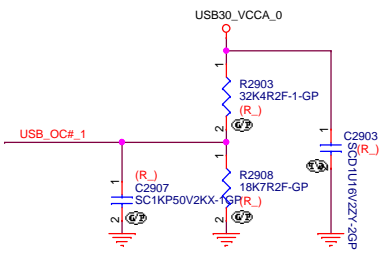
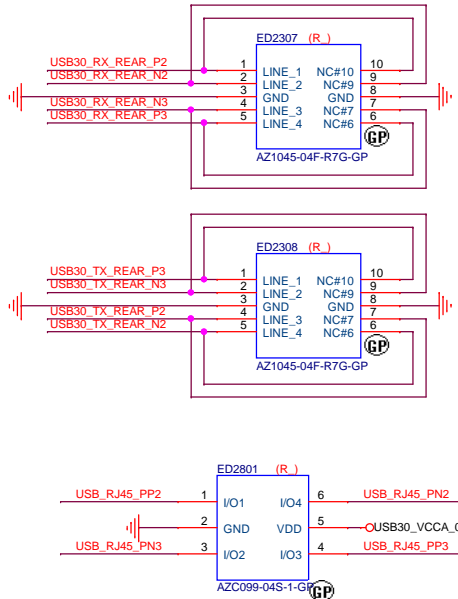
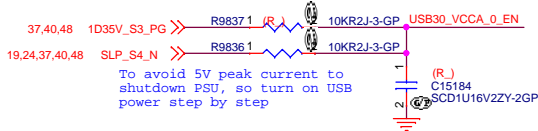
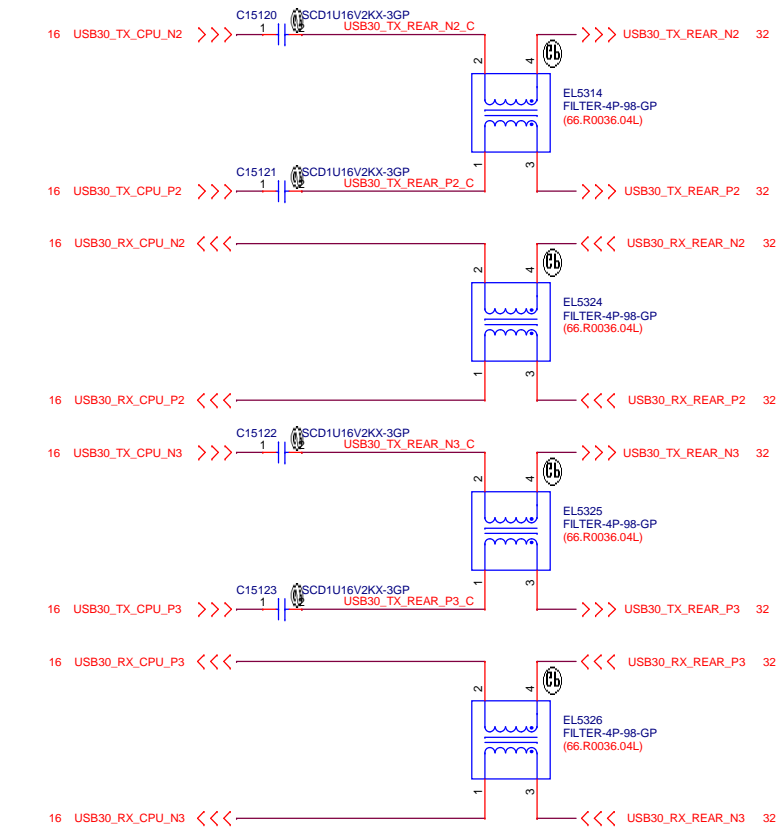
## For USB2F1 (Card Reader)



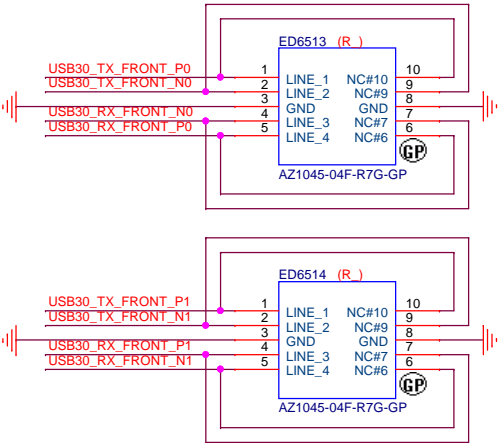
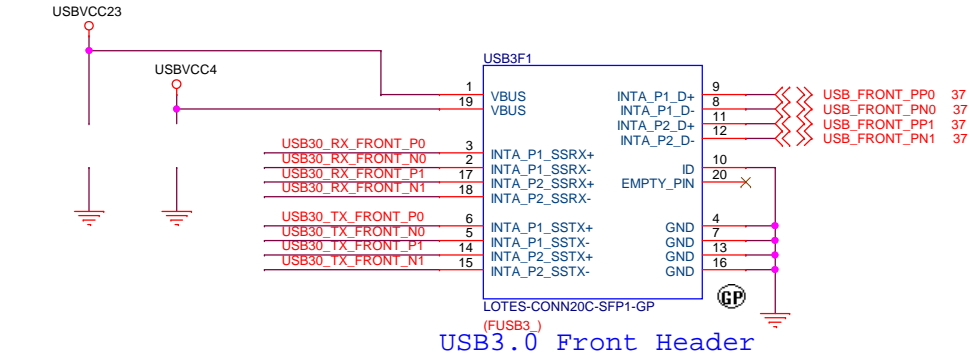
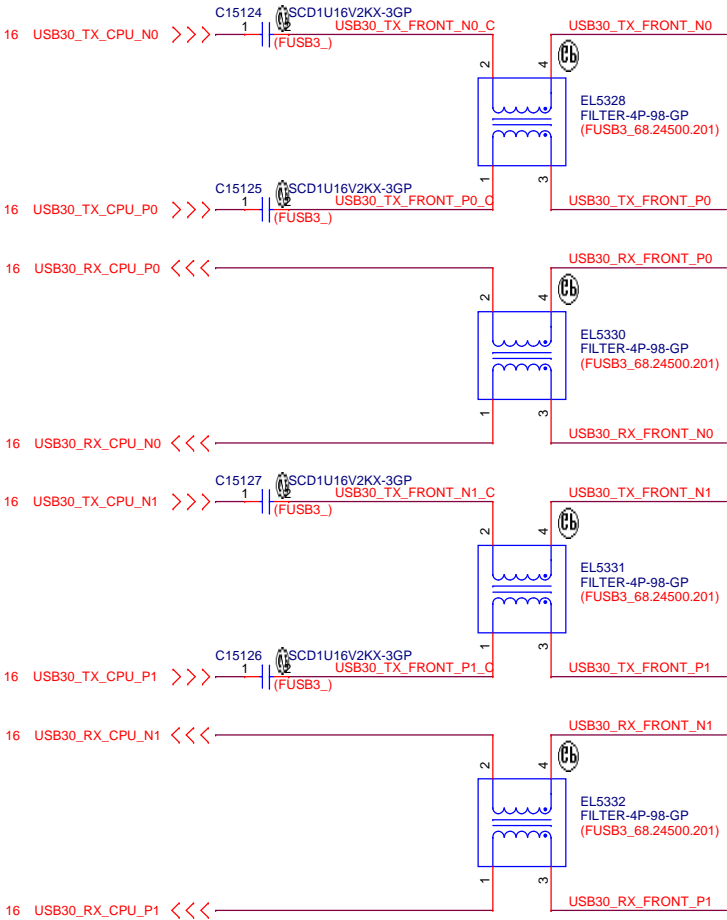
## FP Header USB2.0



# USB 3.0 Rear Port

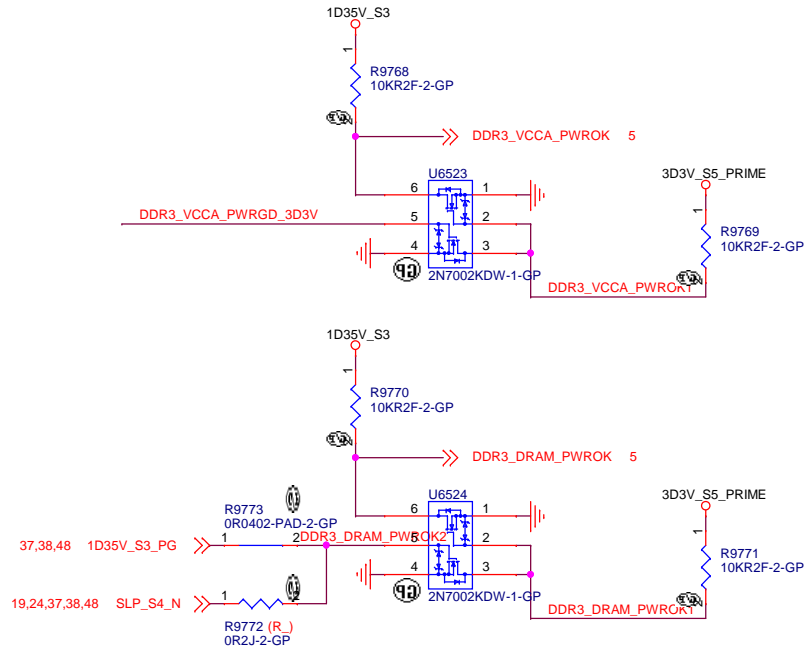
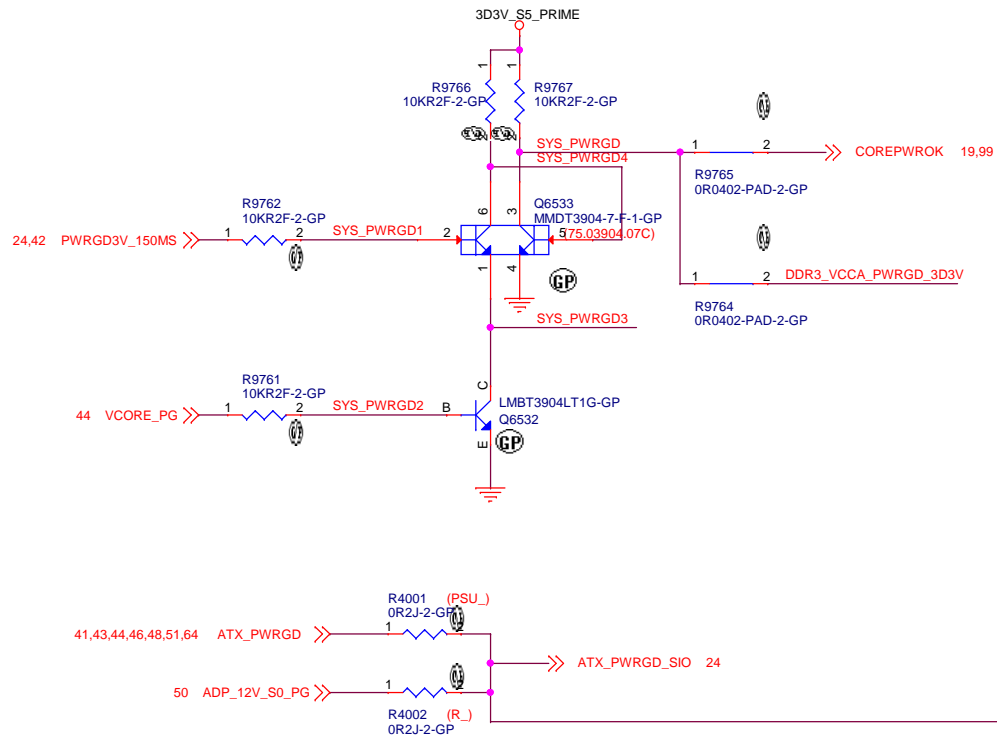


# USB 3.0 Front Port

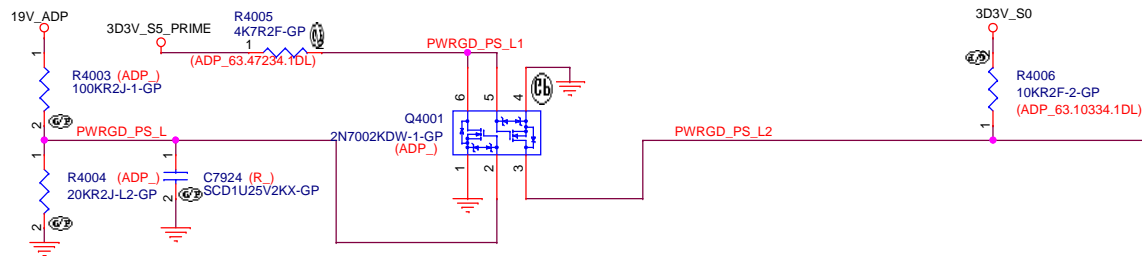


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Hsichih, Taipei Hsien

Title			USB3.0 conn		
Size			Document Number		
B			Braswell		
Date:			Tuesday, April 07, 2015		
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Rev			SA		



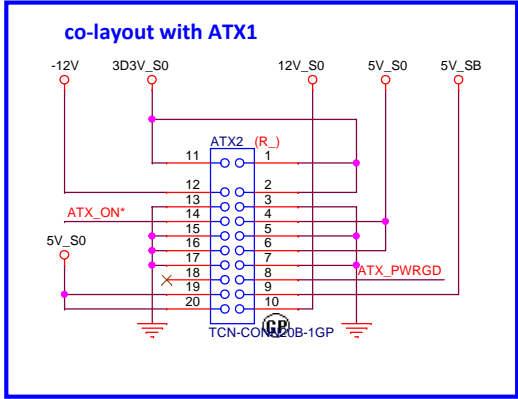
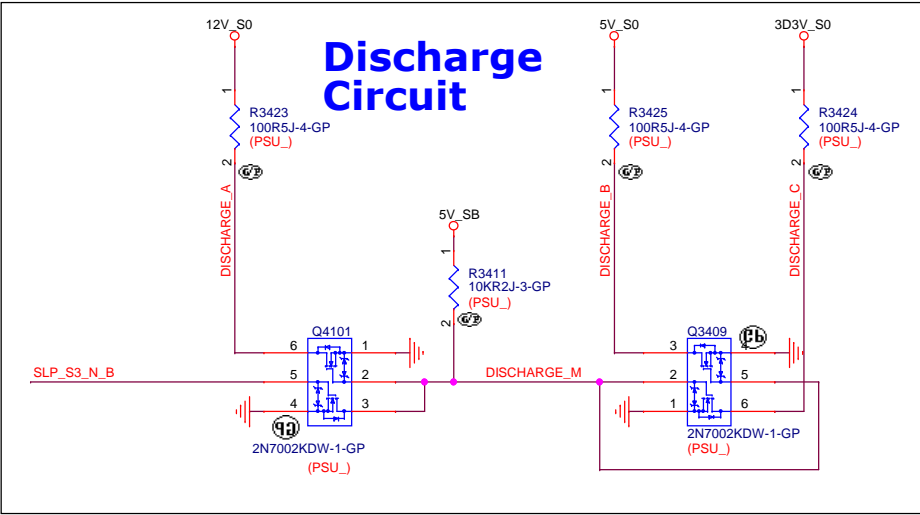
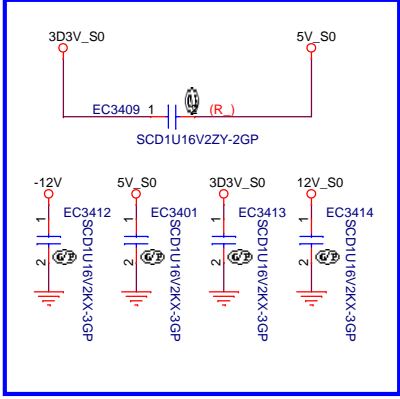
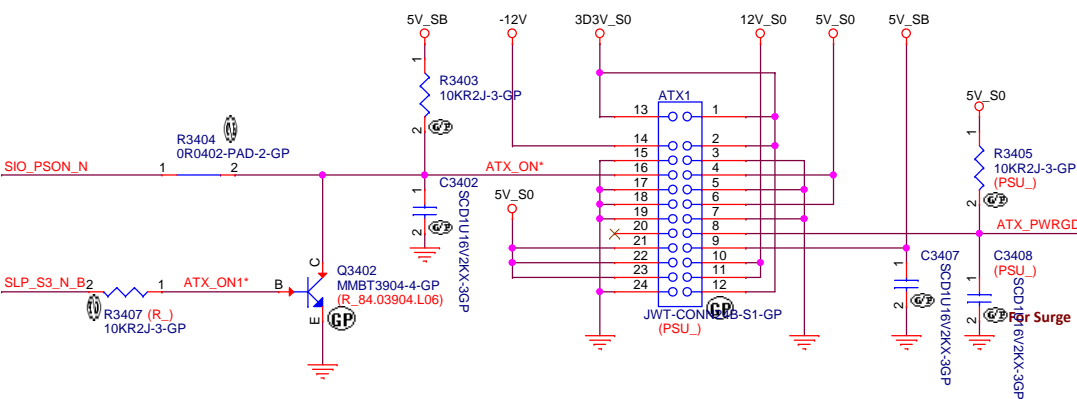
## For AC OFF SEQUENCE



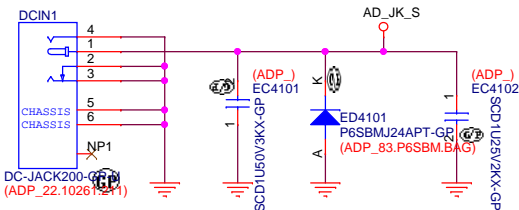


19,24,43,48,50,51 SLP\_S3\_N\_B >>>  
 24,50,54 SIO\_PSON\_N >>>  
 40,43,44,46,48,51,64 ATX\_PWRGD <<<

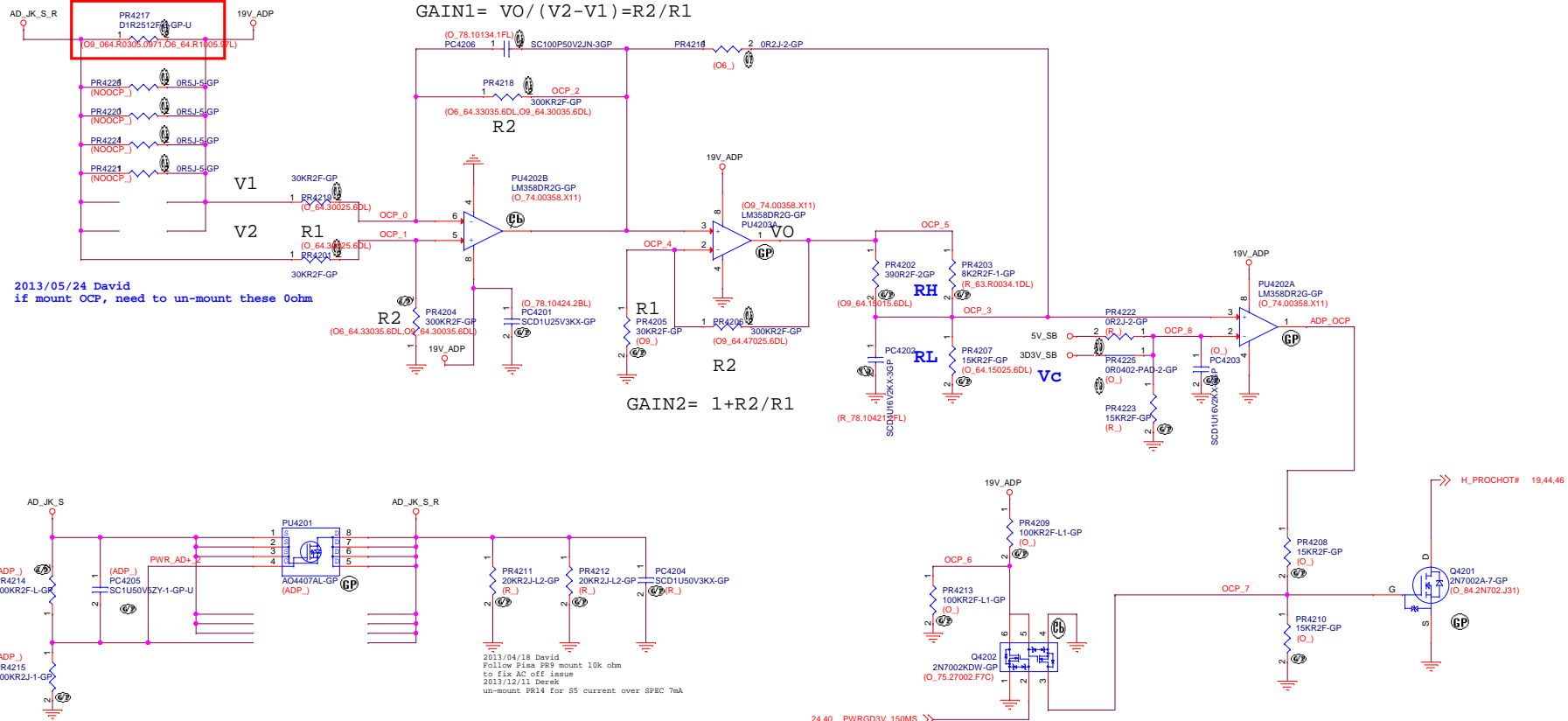
# ATX CONNECTOR



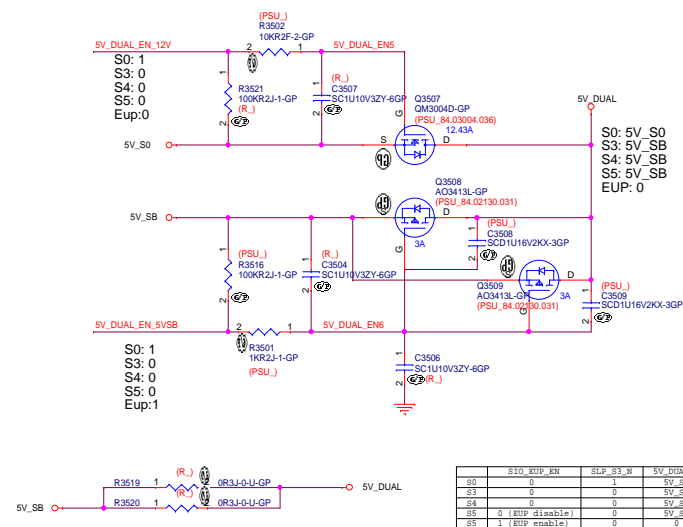
# DC Jack



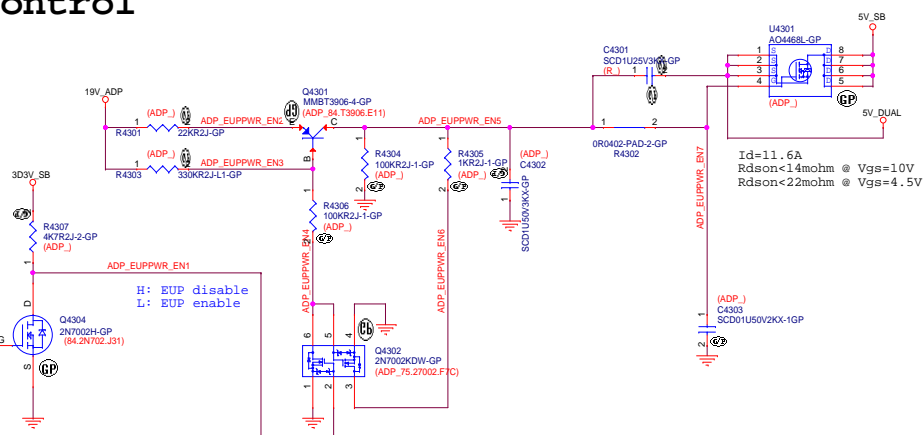
**SIZE 2512  
0.010HM 2W**



## 5V\_DUAL



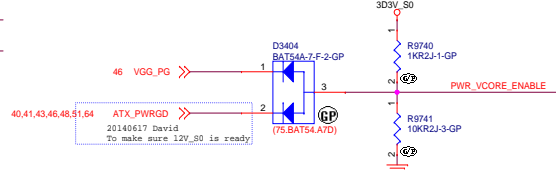
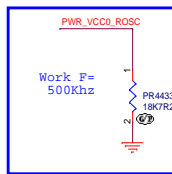
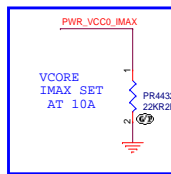
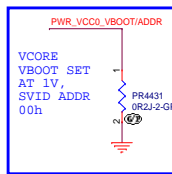
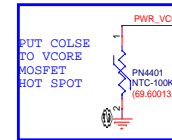
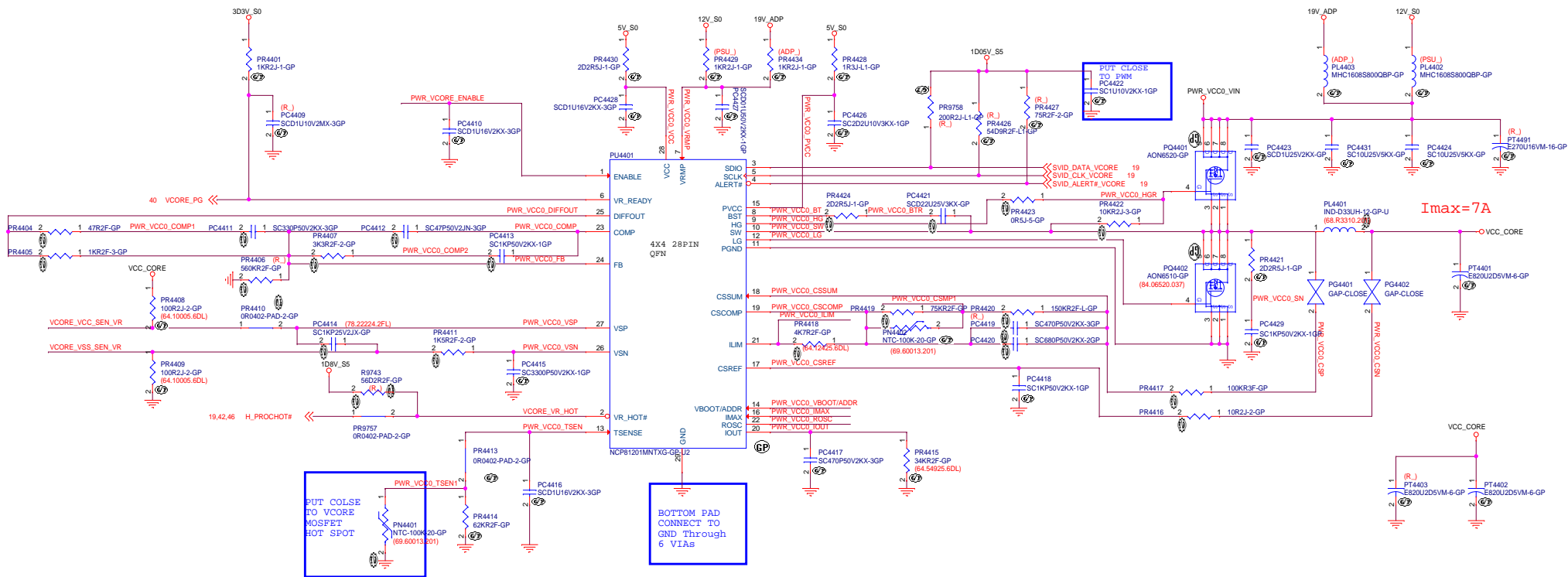
```
3D3V(S5) device:
  SoC
  SIO
  LAN
  WLAN
  PCIe16
```



Id=11.6A  
Rdson<14mohm @ Vgs=10V  
Rdson<22mohm @ Vgs=4.5V

12V\_S0 -> VCC\_CORE

# VR12.1 POWER CKT - 1 phase 12Vin




SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

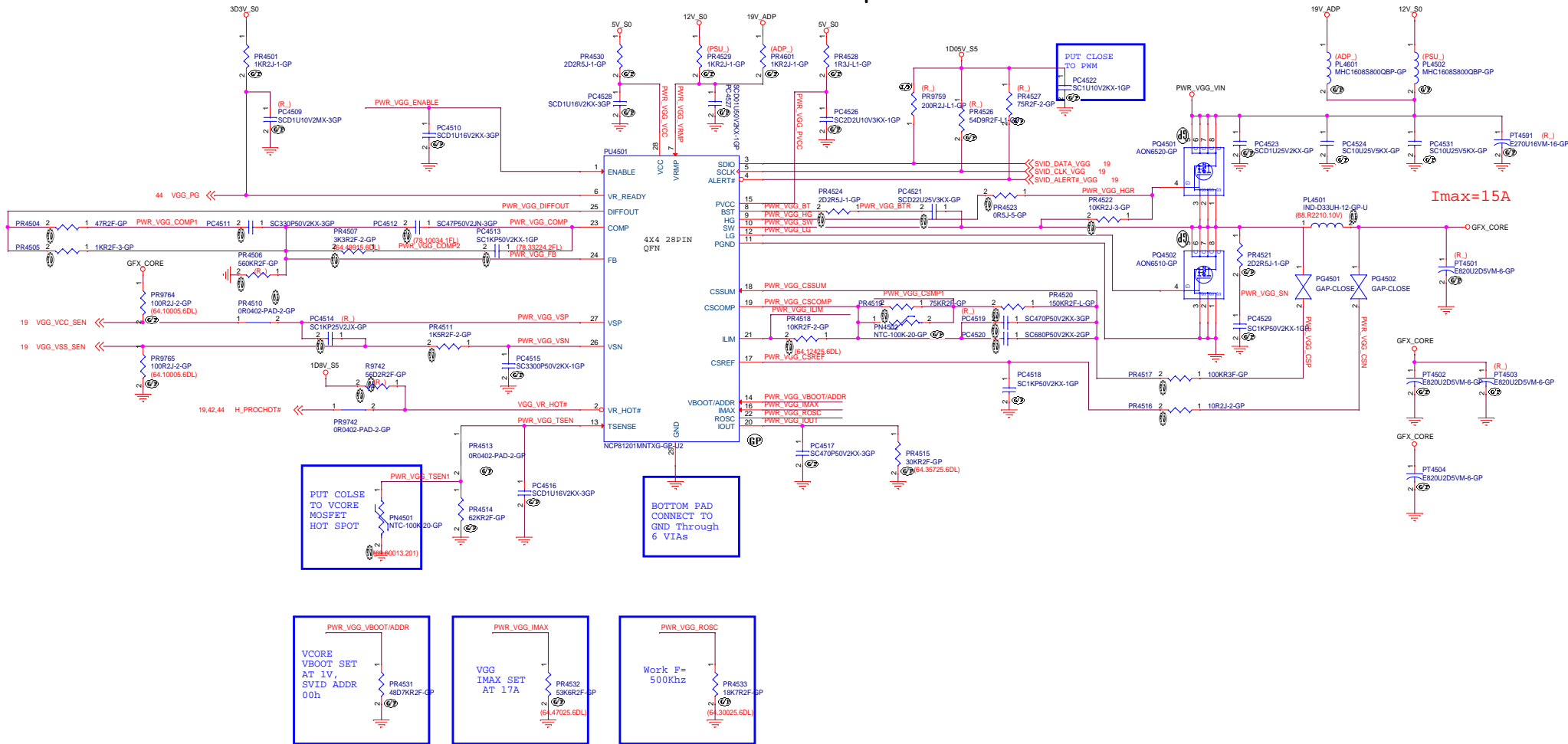
<Variant Name>

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>CPU Core2 (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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12V\_S0 -> GFX\_CORE

# VR12.1 POWER CKT - 1 phase 12Vin

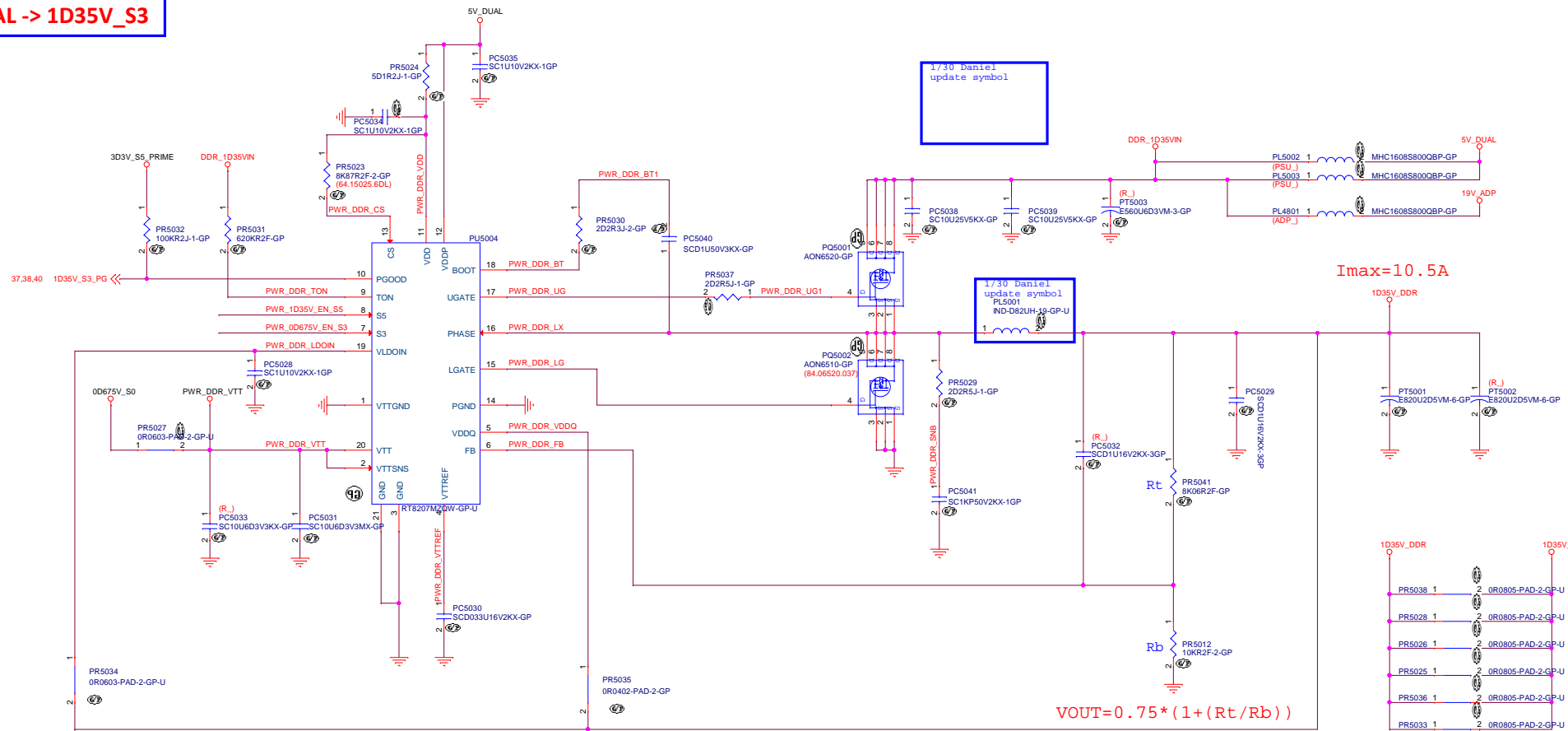


SVID Address and Boot Voltage Table

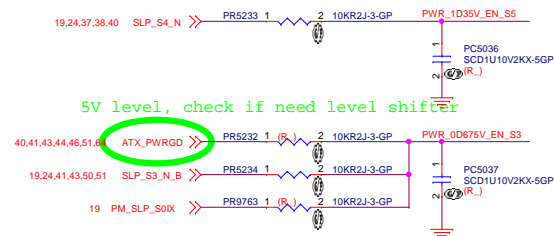
VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x9	1.1
100 k	953	1007	1062	0xA	1.1
113 k	1062	1125	1188	0xB	1.1
124 k	1188	1250	1312	0xC	1.1
137 k	1312	1378	1445	0xD	1.1
150 k	1445	1511	1578	0xE	1.1
165 k	1578	1648	1719	0xF	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1



5V\_DUAL -> 1D35V\_S3



## ENABLE SIGNAL





19V\_A -> 3D3V\_A/5V\_A

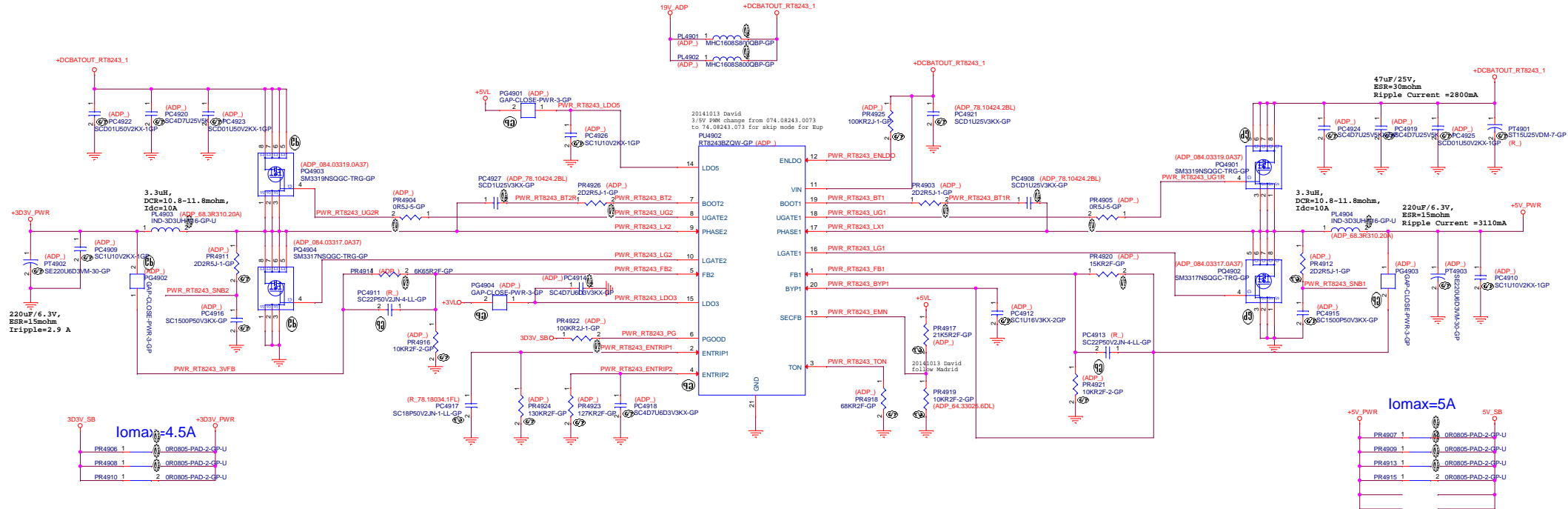
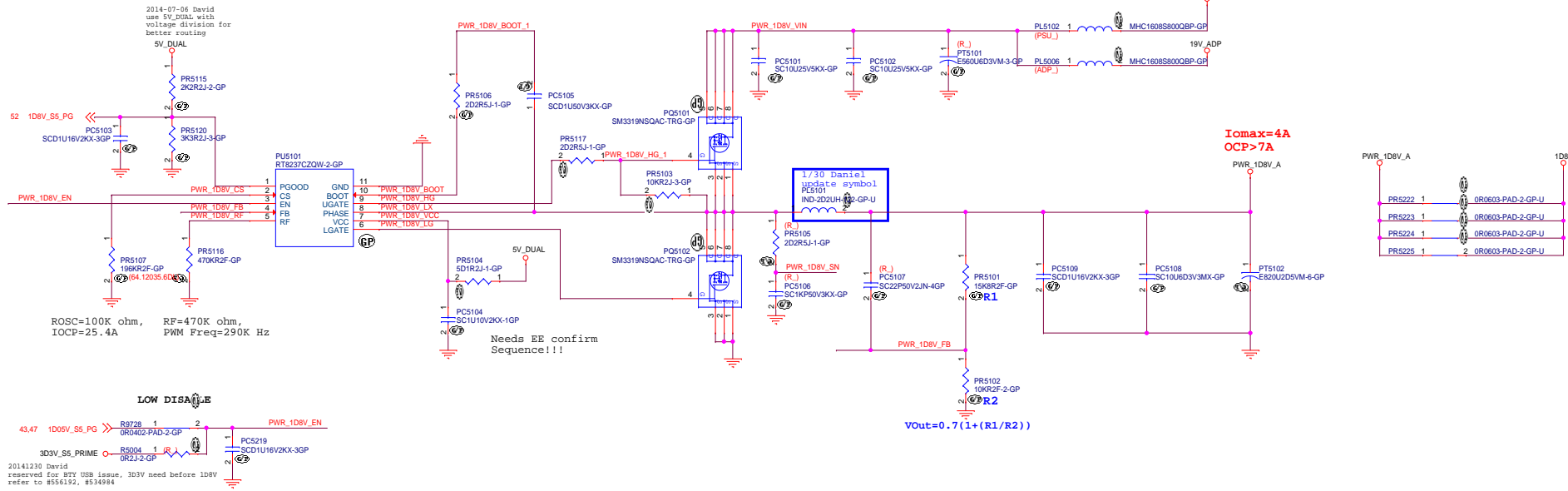


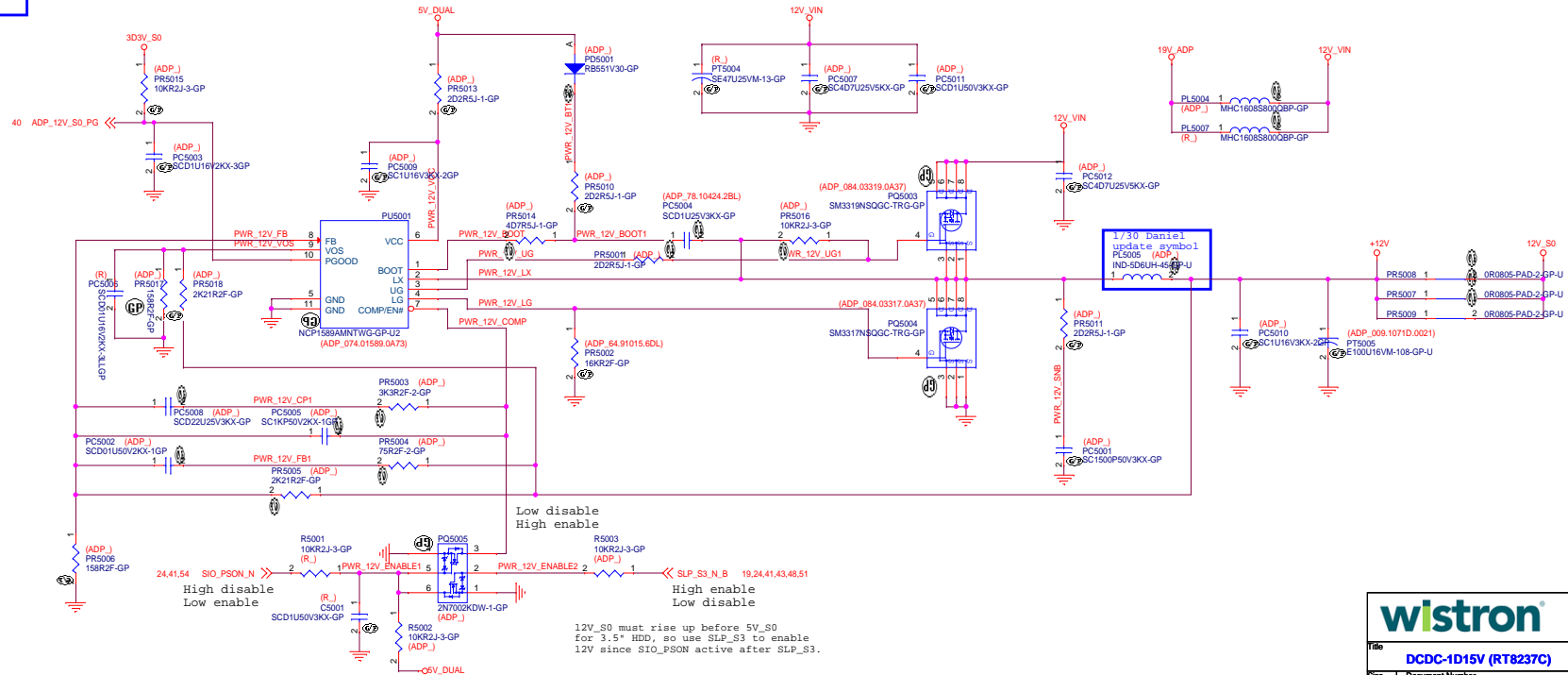
Table 2. Power Up Sequencing(RT8243A)							
ENLDO(V)	ENM	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMP51	SMP52
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

## 5V\_DUAL -> 1D8V\_S5

VIN RIPPLE CURRENT  $I_{max}=1.94A$



## 19V\_A -> 12V\_S0



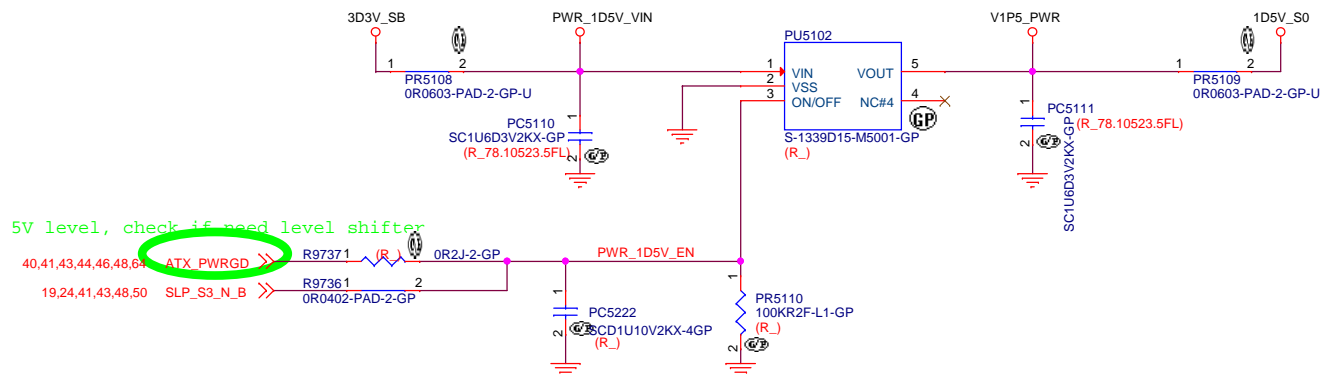
## 3D3V\_SB -> 1D5V\_S0

Iomax=0.42A

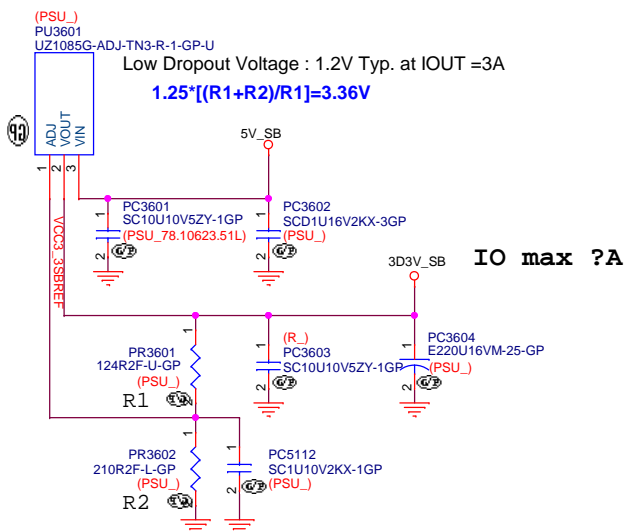
$$PD = (V_{in} - V_{out}) * I_{omax}$$

$$= (3.3 - 1.5) * 0.025A = 0.045W$$

I<sub>max</sub>=0.025A



## 5V\_SB -> 3D3V\_SB



**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title  
**LDO-1D5V (APL5930)**

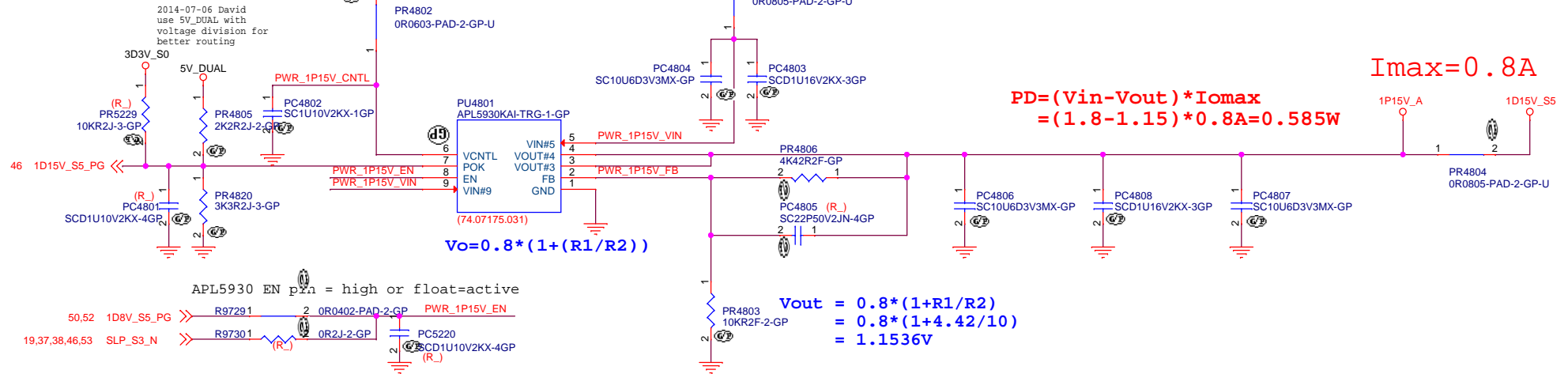
Size B  
Document Number  
**Braswell**

Rev  
SA

Date: Tuesday, April 07, 2015 Sheet 51 of 111

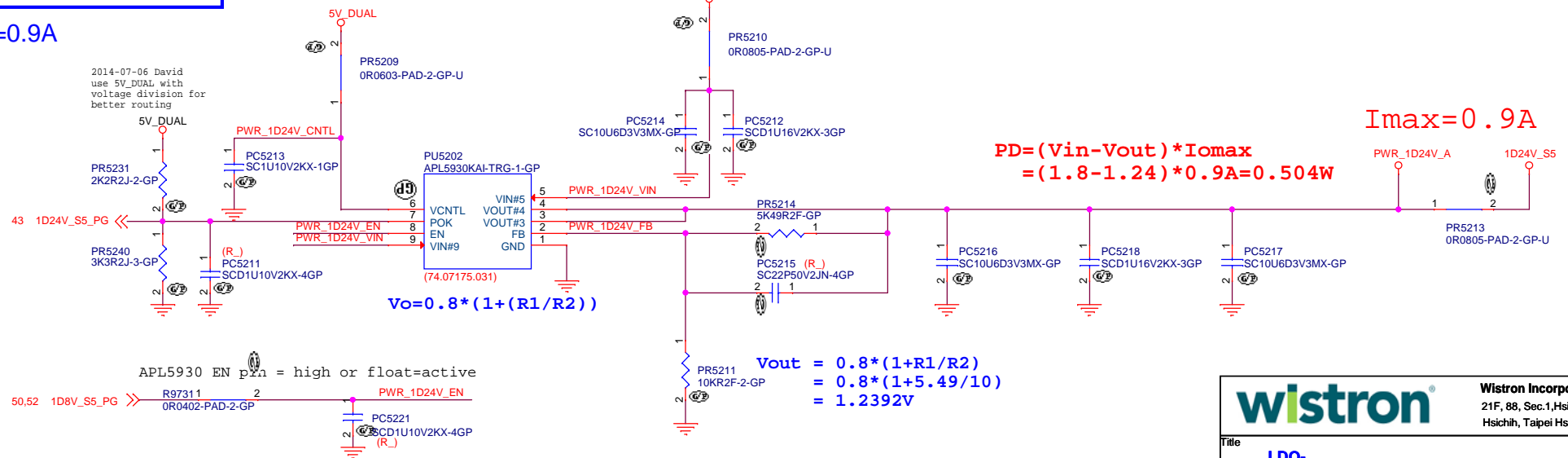
## 1D8V\_S5 -> 1D15V\_S5

I<sub>max</sub>=0.8A



## 1D8V\_S5 -> 1D24V\_S5

I<sub>max</sub>=0.9A

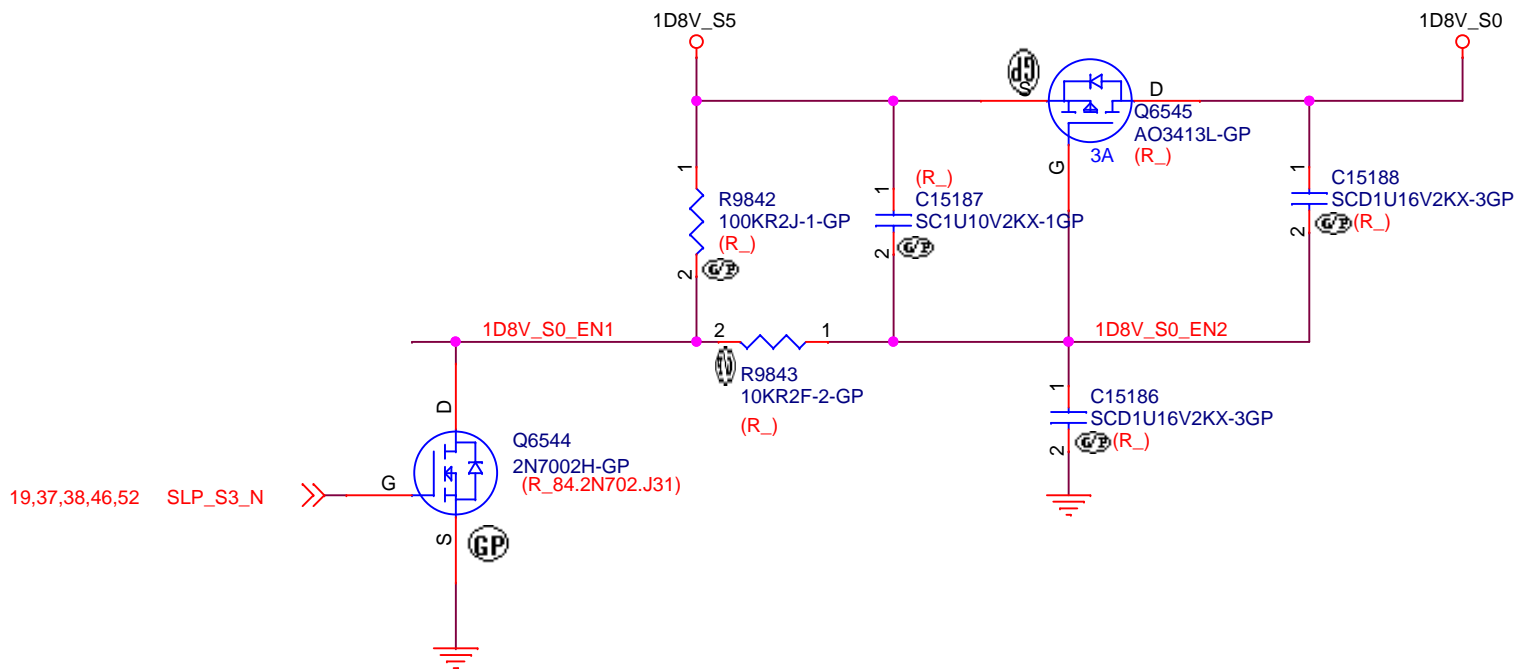


**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title		LDO-	
Size	Document Number	Braswell	
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Date:	Thursday, April 09, 2015	Sheet	52 of 111

1D8V\_S5 -> 1D8V\_S0



**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title

**Switch power-1D8V (RT8068A)**

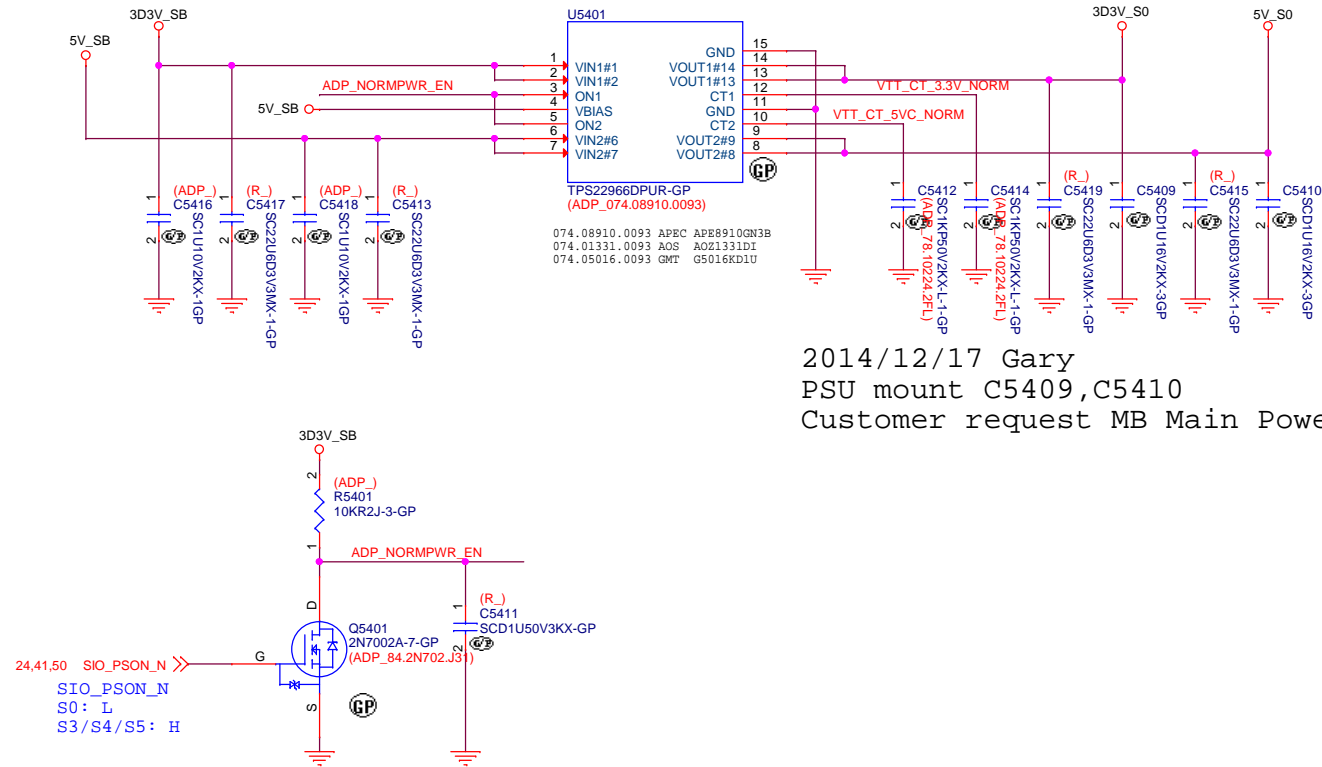
Size  
A

Document Number  
**Braswell**

Rev  
SA


Date: Tuesday, March 24, 2015

Sheet 53 of 111

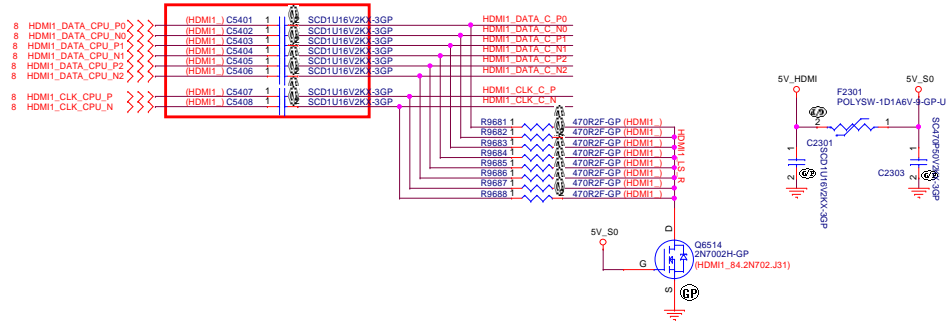


	5	4	3	2	1
D					
C					
B					
A					

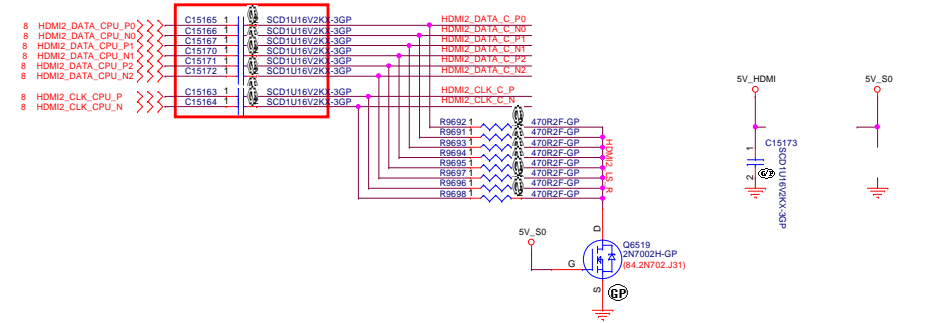
(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>LVDS/Converter (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 55 of 111	

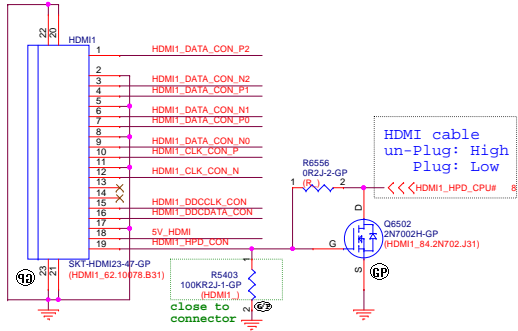
### Close to HDMI Connector



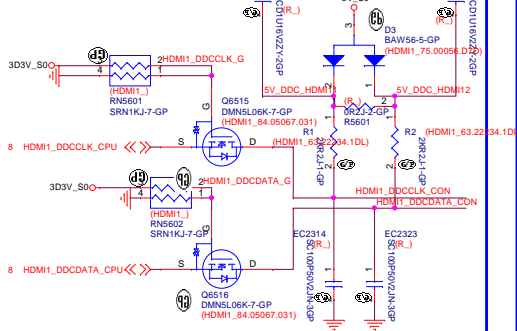
### Close to HDMI Connector



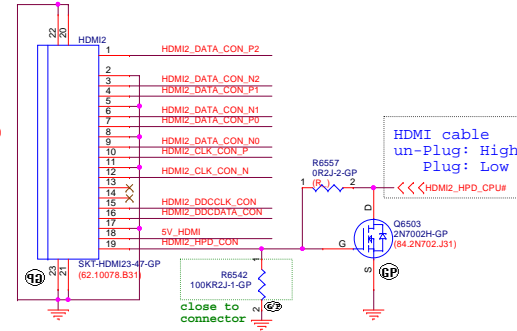
### HDMI1 CONN



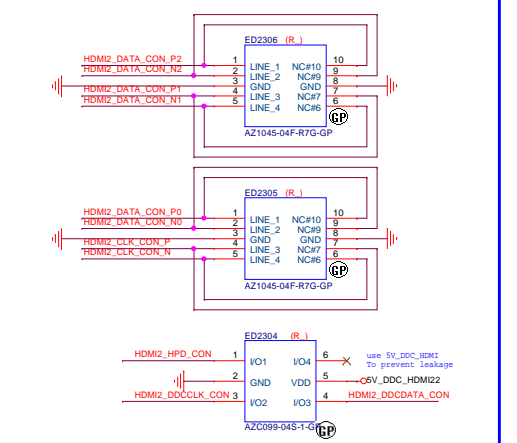
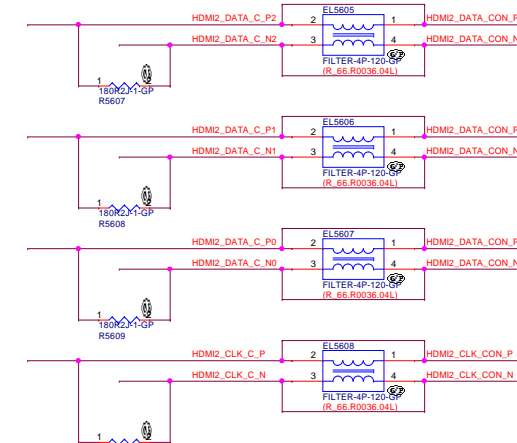
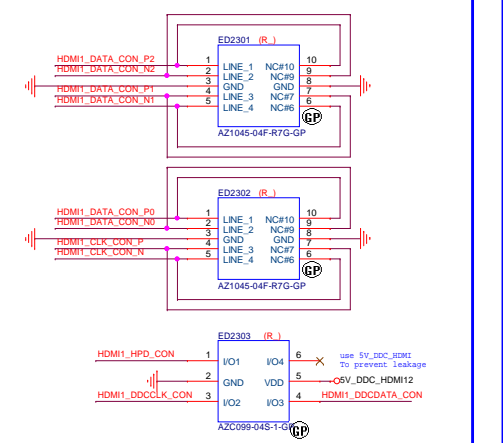
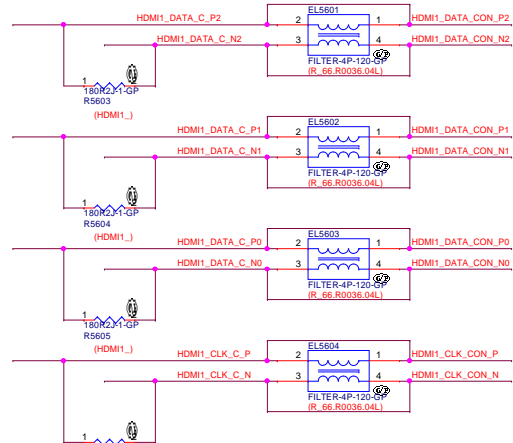
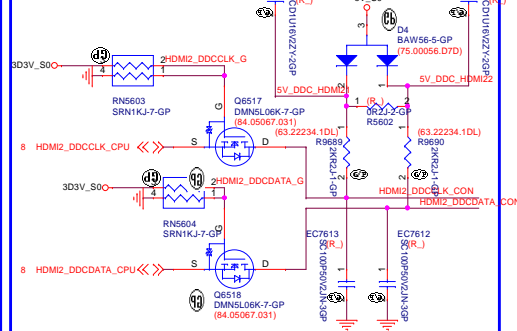
### DDC Level Shifter



### HDMI2 CONN




### DDC Level Shifter





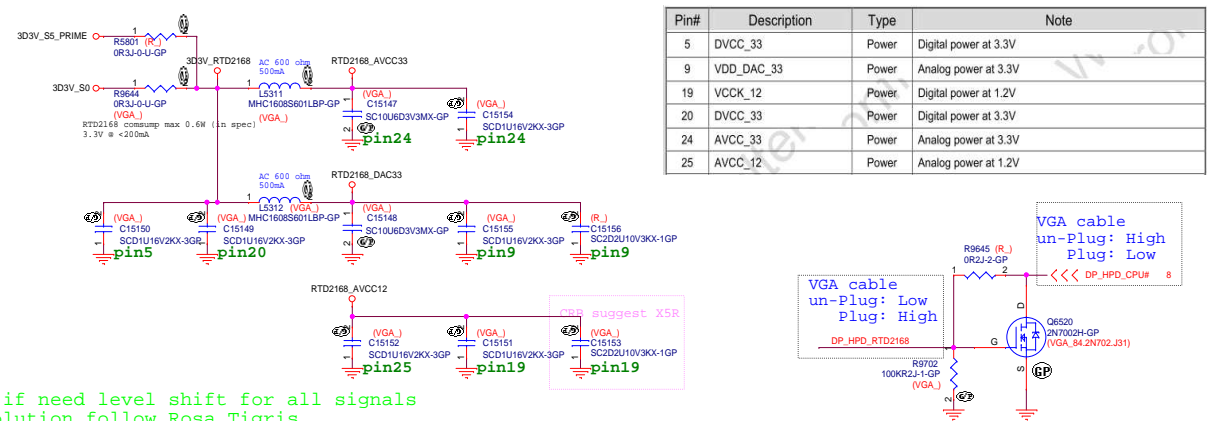
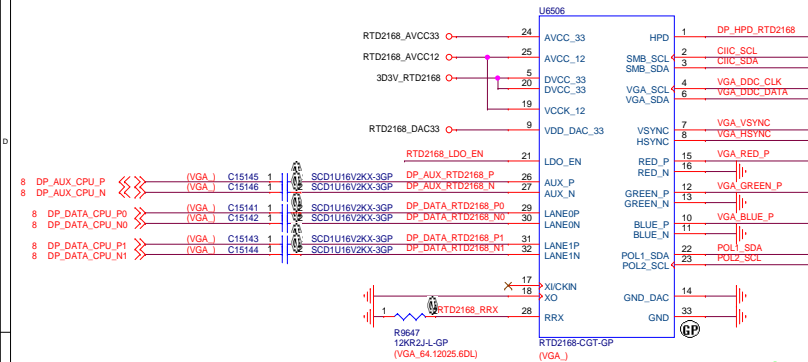
	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>DP/eDP (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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# DP to VGA converter: RTD2168

Pin#	Description	Type	Note
5	DVCC_33	Power	Digital power at 3.3V
9	VDD_DAC_33	Power	Analog power at 3.3V
19	VCCK_12	Power	Digital power at 1.2V
20	DVCC_33	Power	Digital power at 3.3V
24	AVCC_33	Power	Analog power at 3.3V
25	AVCC_12	Power	Analog power at 1.2V



①. Check if need level shift for all signals  
②. ESD solution follow Rosa Tigris

## Mode Configure Table(Power On Latch)

	POL1_SDA(PIN22)	
	0	1
POL2_SCL(PIN23)	0	X
	1	ROM ONLY MODE
		EEPROM MODE

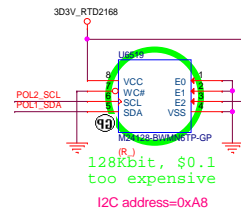
RTD2168 Supports three operation mode for system design. Reserve 4.7K resistor pull high/low for mode selection.

ROM ONLY Mode : PIN22 pull low, PIN23 pull high  
EP Mode : PIN22 pull high, PIN23 pull low  
EEPROM Mode : PIN22 pull high, PIN23 pull high

## EEPROM MODE

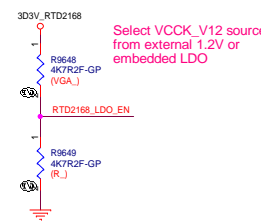
In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following conditions.

- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



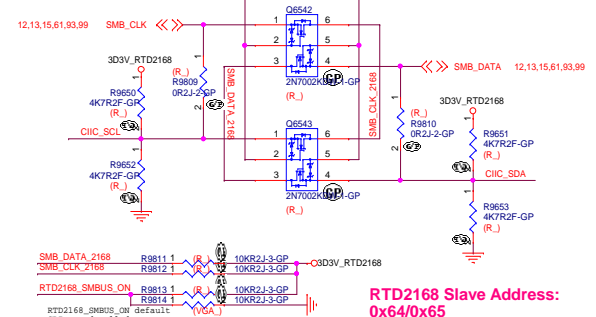
## Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

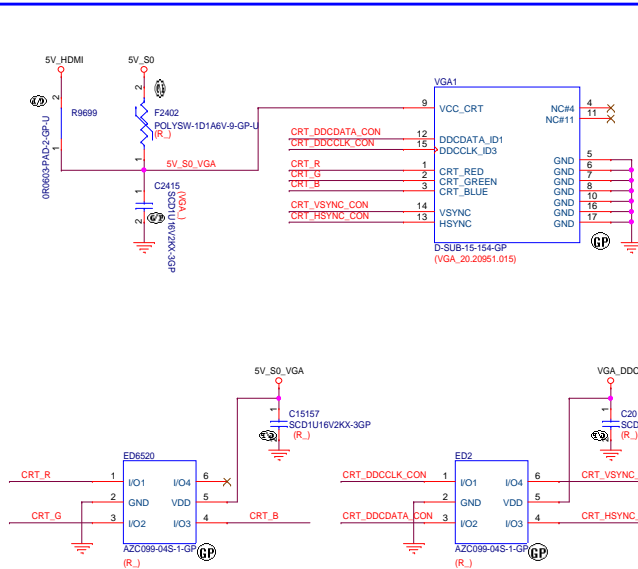
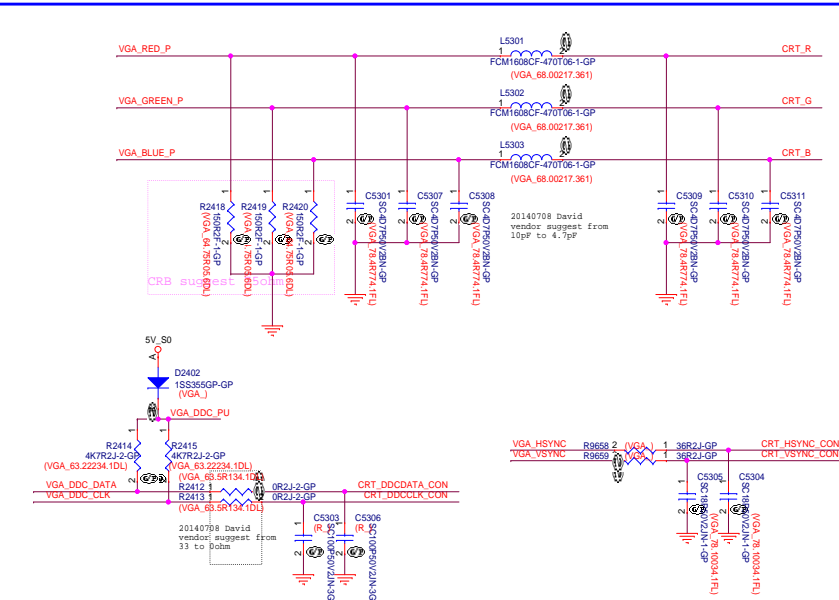


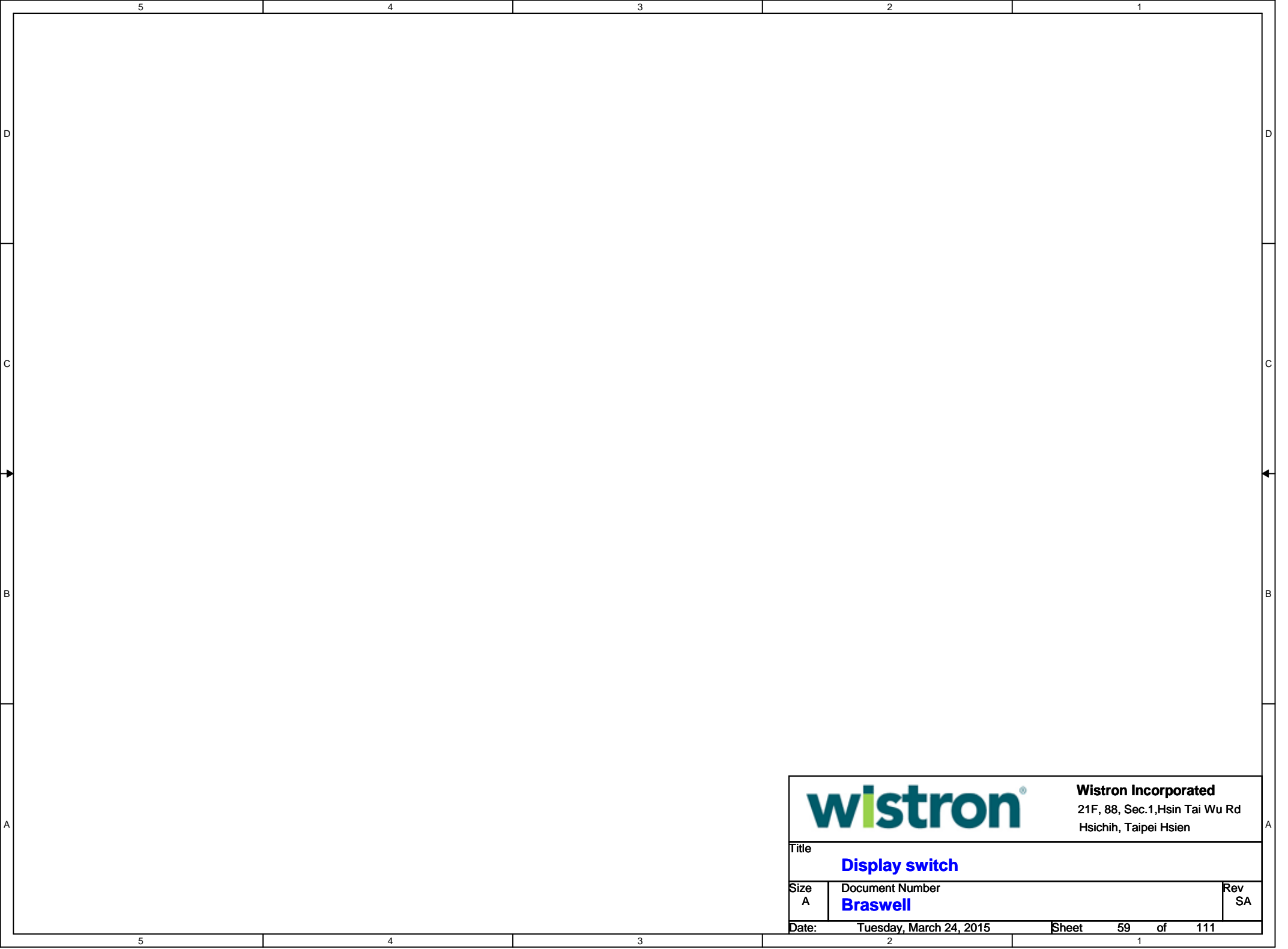
## EP Mode


Pin2, Pin3 should be connected to EC for EP mode I2C protocol is used

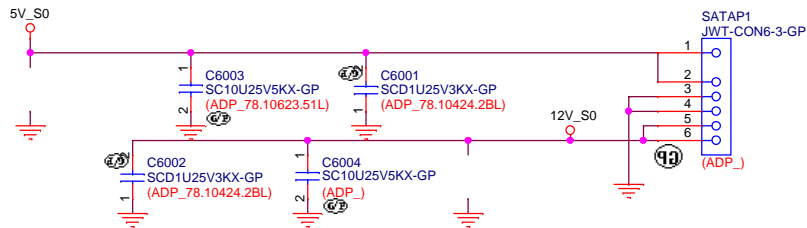
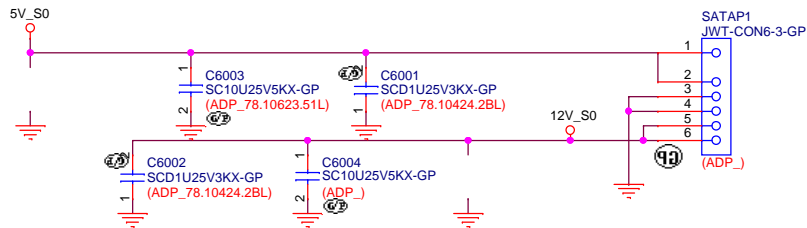
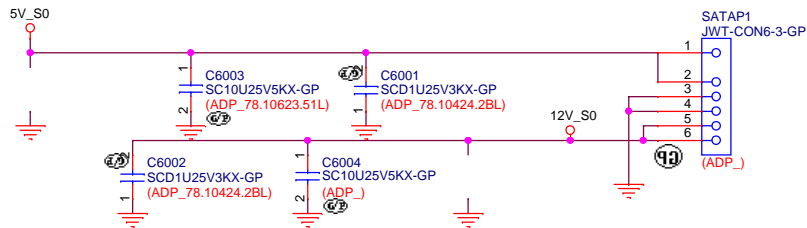
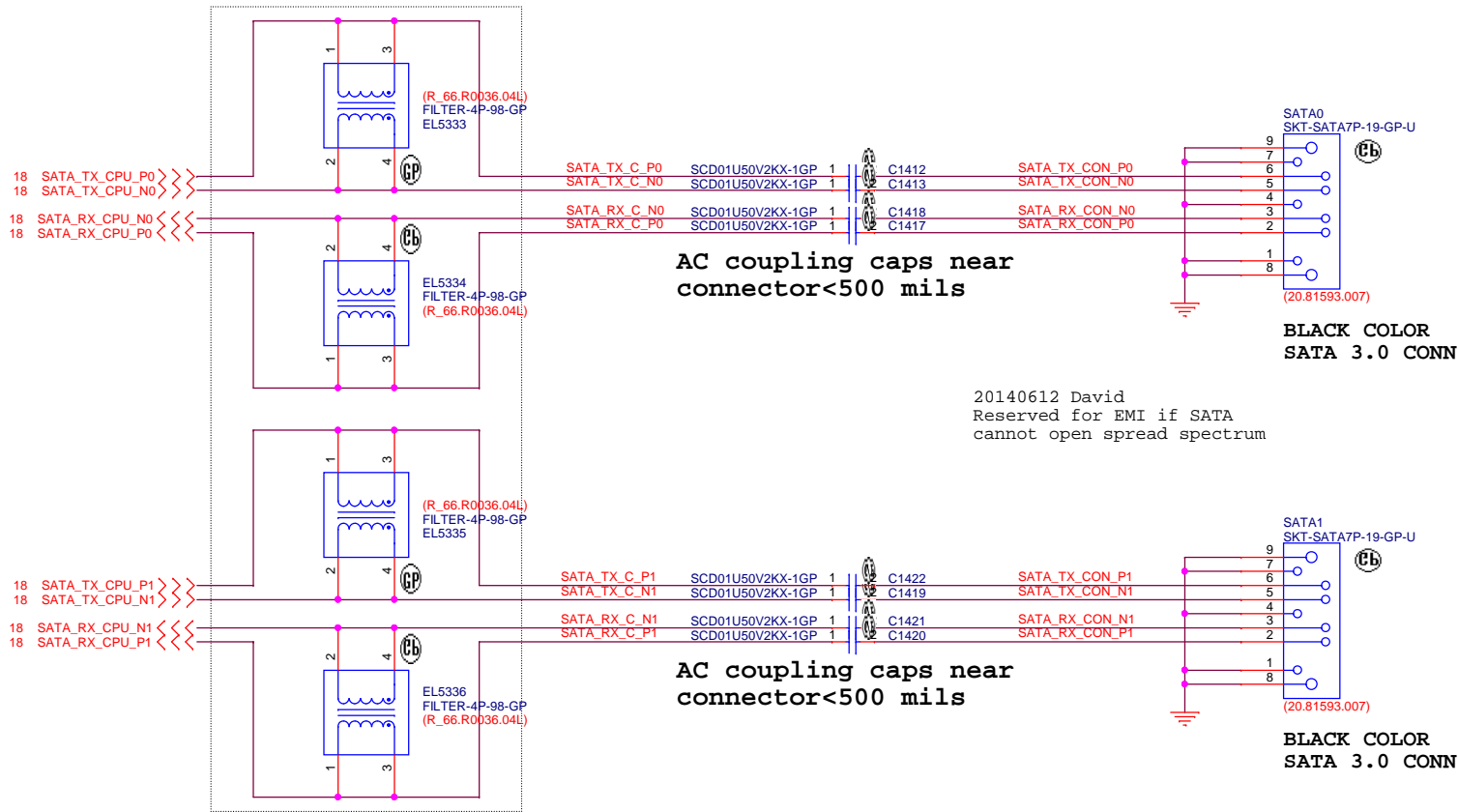


RTD2168 Slave Address: 0x64/0x65

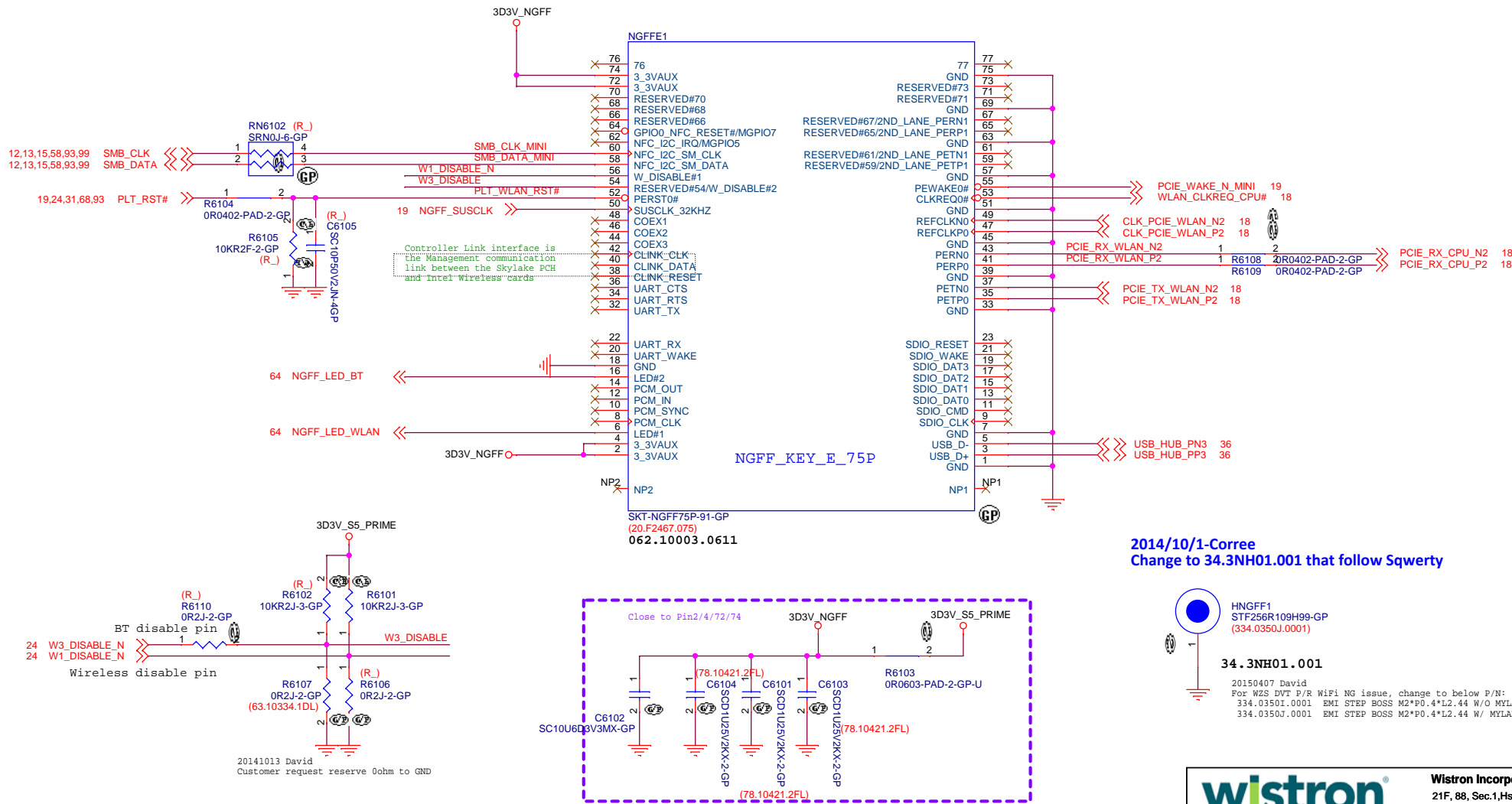




		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Display switch</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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# M.2 2230 / 1630 Key E Type (Wireless LAN+BT)




HNGFF1  
STF256R109H99-GP  
(334.0350J.0001)

**34.3NH01.001**

20150407 David  
For W2S DVT P/R WiFi NG issue, change to below P/N:  
334.0350I.0001 EMI STEP BOSS M2\*P0.4\*L2.44 W/O MYLAR  
334.0350J.0001 EMI STEP BOSS M2\*P0.4\*L2.44 W/ MYLAR


	5	4	3	2	1
D					
C					
B					
A					

(Reserved)

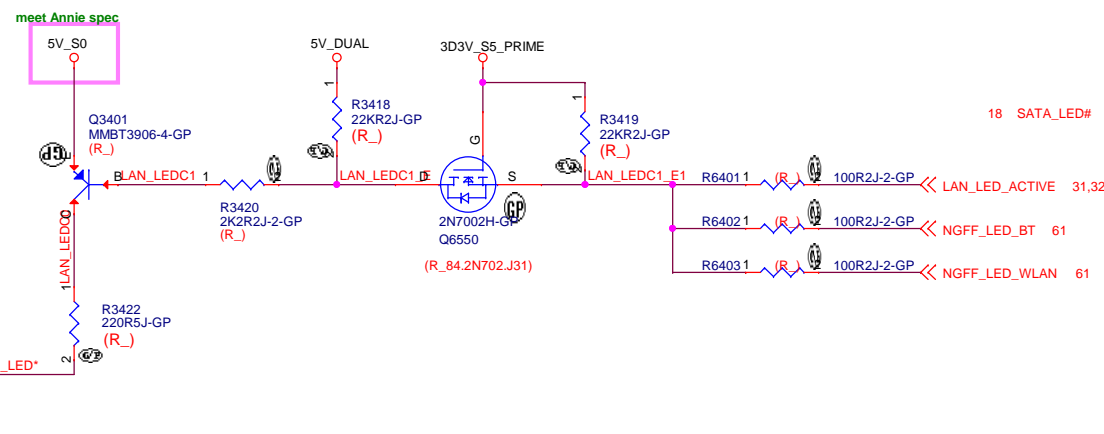
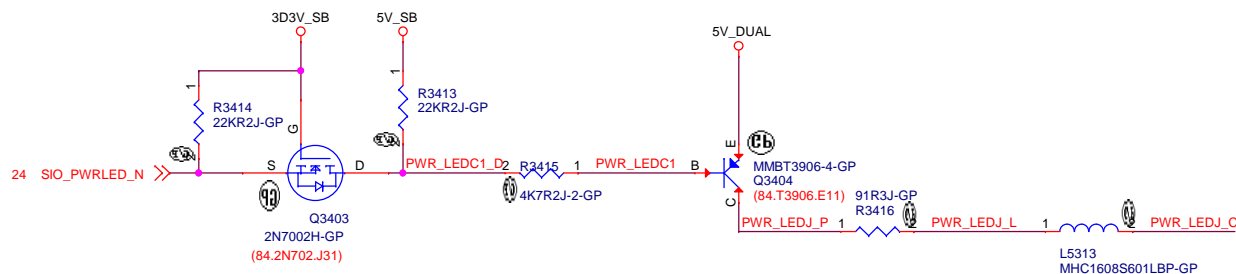
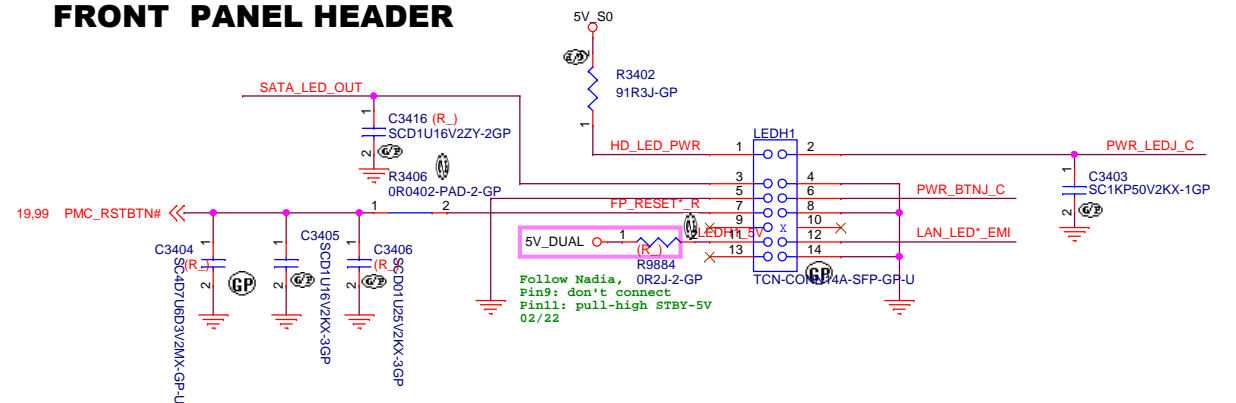
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Mini card-SSD/TV (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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	5	4	3	2	1
D					
C					
B					
A					

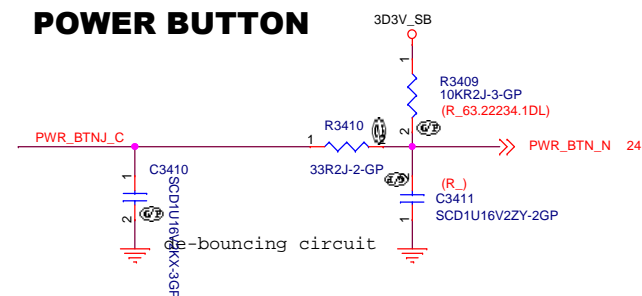
(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Mini card-NGFF (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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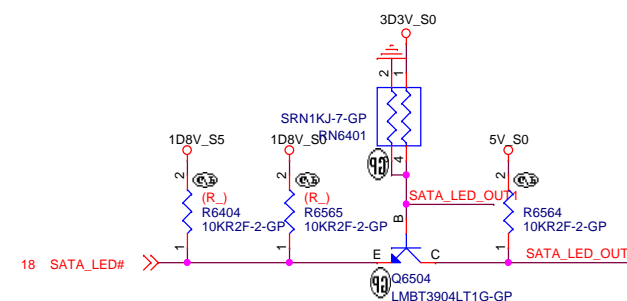
## FRONT PANEL HEADER



## POWER BUTTON




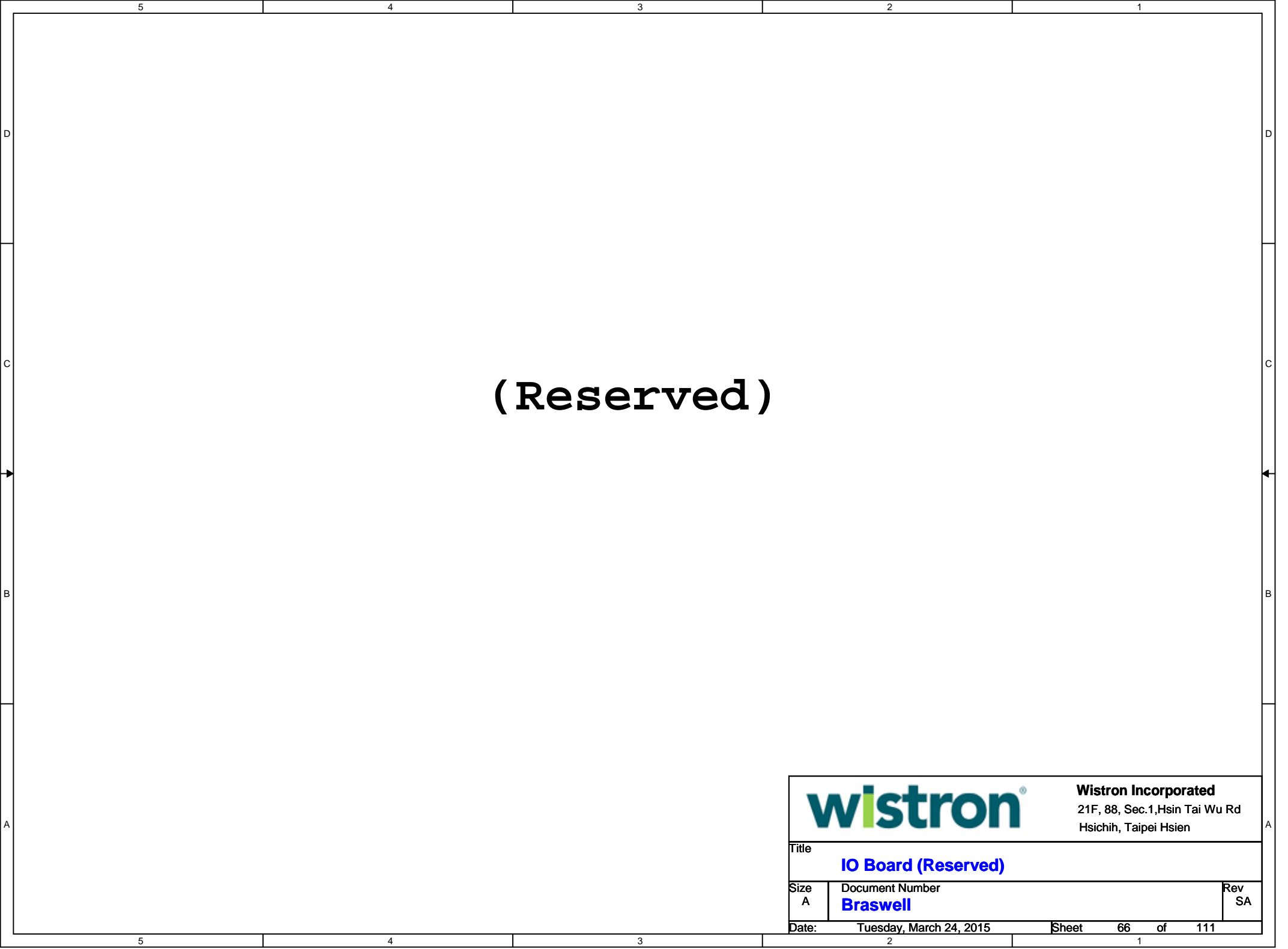
0118 Reserve for AMD's suggestion  
0224 Delete due to layout did not add






(Reserved)

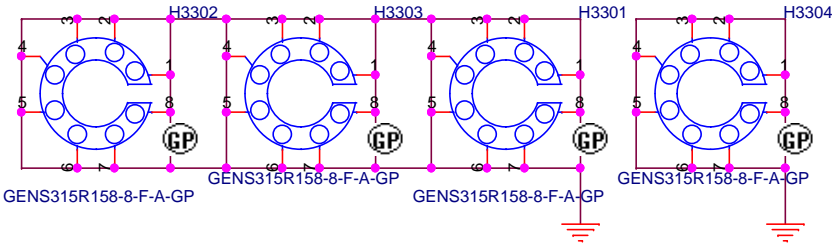
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>(Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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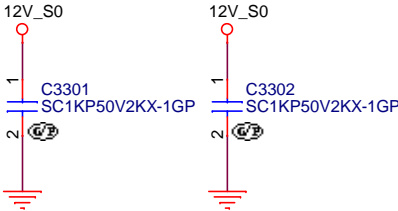
(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>IO Board (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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Scrc Hole (PCB New type MOUNTING HOLES)



Bogis 20130826  
Del R3301  
Connect H3304 from ESDGND to GND



LABEL



LBL1  
LABEL  
(45.41107.021)

45.41107.011 (一般的紙, 70x8mm過完高溫reflow之後會變的偏黃)  
45.41101.001 (一般的紙, 35x15mm, 過完高溫reflow之後會變的偏黃)  
40.3KP03.001 (高溫貼紙, 35x15mm, 過完高溫reflow之後紙還是很白)



LBL2  
LABEL  
(R\_45.41101.011)

2015/02/02 WZS's request  
35x15 (40.3KP03.011)  
30x15 (40.3BZ24.011)  
70x8 (45.41107.021)



LBL3  
LABEL  
(R\_40.3KP03.001)

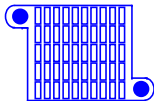
Battery Symbol



BAT1  
BATTERY CR2032  
(23.20068.001)

23.20068.001 KTS BBBCR2032BX  
23.20023.311 MITSUBISHI CR2032 MITSUBISHI  
23.22063.001 JHT CR2032 JHT

HeatSink Symbol



CPUHS1  
HEATSINK  
(360.02201.0021)

Brian 10W  
P/N:  
360.02201.0001 60.3ET05.001  
360.02201.0011 60.3ET05.011  
360.02201.0021 60.3ET05.021

Vendor  
P/N:

14044-SA PCB  
48.N0077.0SA

14074-SA PCB  
348.02202.00SA  
348.02203.00SA  
348.02204.00SA

PCB No.: 14074  
PCB Version: SB  
348.02202.00SB  
348.02203.00SB  
348.02204.00SB

GLOBALBRAN (Yes)  
TRUSTECH (Yes)

PCB No.: 14074  
PCB Version: SC  
348.02203.00SC  
348.02204.00SC  
348.02207.00SC

GLOBALBRAN  
TRUSTECH  
VICTORYGIA

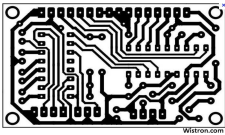
PCB No.: 14074  
PCB Version: 1A  
348.02203.001A  
348.02204.001A  
348.02207.001A

GLOBALBRAN  
TRUSTECH  
VICTORYGIA

PCB No.: 14074  
PCB Version: -1  
348.02203.0011  
348.02204.0011  
348.02207.0011

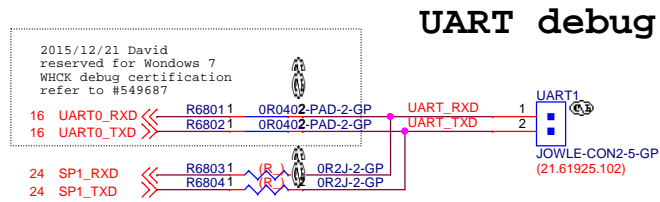
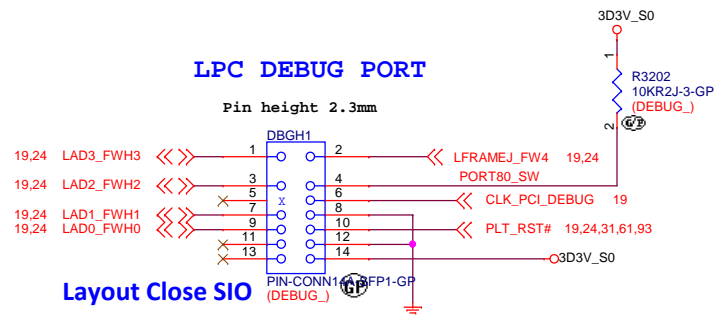
GLOBALBRAN  
TRUSTECH  
VICTORYGIA

PCB Symbol




PCB1  
PCB  
(348.02203.0011)

		Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Screw Hole</b>			
Size	Document Number		Rev
Custom	<b>Braswell</b>		SA
Date:	Thursday, April 09, 2015		Sheet 67 of 111




(Reserved)


		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>(Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 69 of 111	

	5	4	3	2	1
D					
C					
B					
A					


(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>G Sensor (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 70 of 111	

(Reserved)


		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Thunderbolt (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)


		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Thunderbolt (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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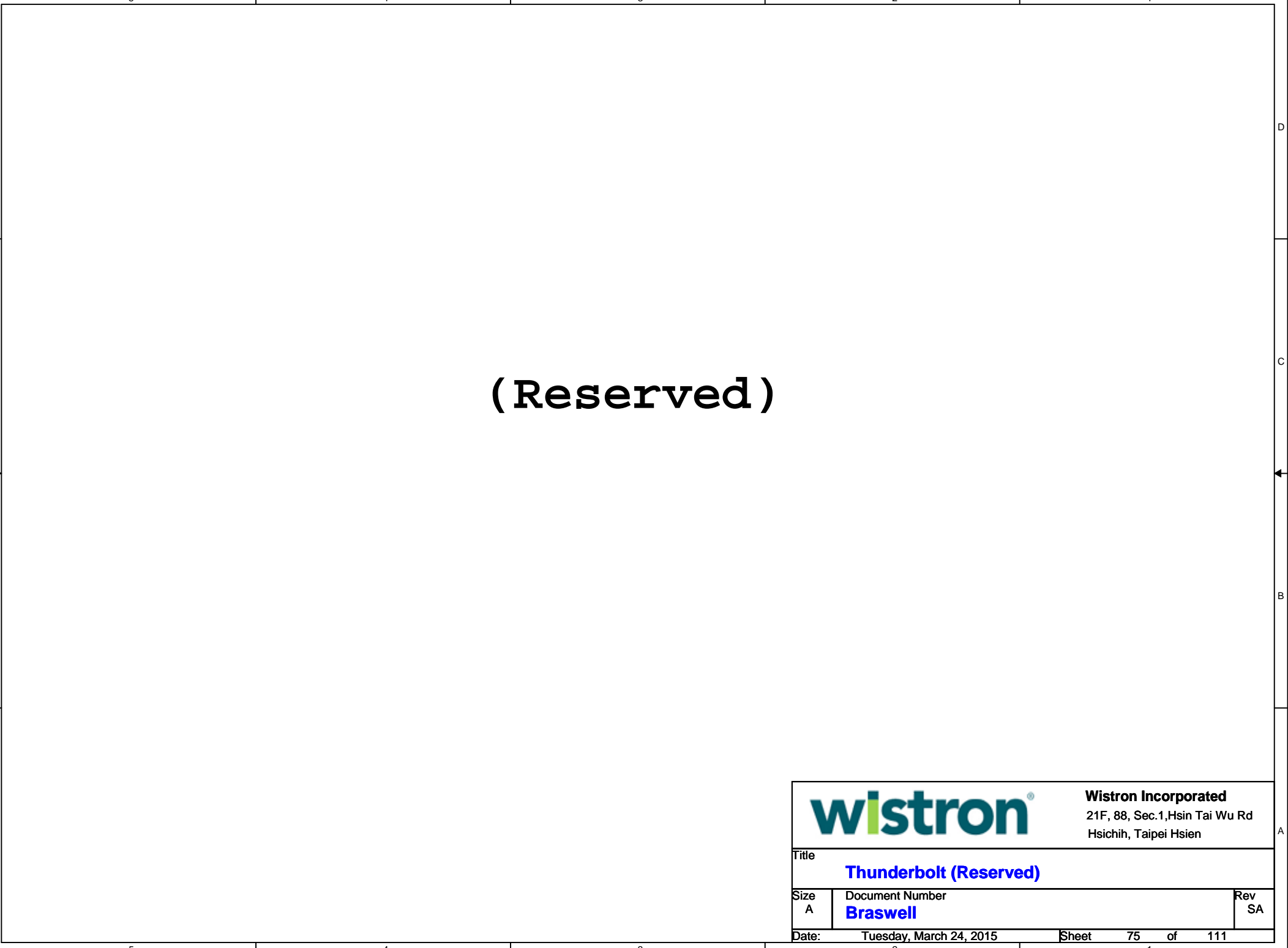


(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Thunderbolt (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Thunderbolt (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	74 of 111




5		4		3		2		1	
D									
C									
B									
A									

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Thunderbolt (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)



Wistron Incorporated

21F, 88, Sec.1,Hsin Tai Wu Rd

Hsichih, Taipei Hsien

Title


GPU (Reserved)

Size A	Document Number Braswell	Rev SA
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Date: Tuesday, March 24, 2015

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(Reserved)




(Reserved)



(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)



Wistron Incorporated

21F, 88, Sec.1,Hsin Tai Wu Rd

Hsichih, Taipei Hsien

Title

GPU (Reserved)


Size A	Document Number Braswell	Rev SA
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Date: Tuesday, March 24, 2015


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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU VRAM 1/2 (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU VRAM 3/4 (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet 82 of 111	


(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU VRAM 5/6 (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU VRAM 7/8 (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU CORE (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	85 of 111

(Reserved)



**Wistron Incorporated**  
21F, 88, Sec.1,Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title

**GPU power (Reserved)**

Size  
A


Document Number  
**Braswell**

Rev  
SA


Date: Tuesday, March 24, 2015

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(Reserved)


		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU Switch (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
Date:	Tuesday, March 24, 2015	Sheet	87 of 111

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>GPU Switch (Reserved)</b>			
Size A	Document Number <b>Braswell</b>		Rev SA
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(Reserved)



Wistron Incorporated

21F, 88, Sec.1,Hsin Tai Wu Rd

Hsichih, Taipei Hsien

Title


GPU others (Reserved)

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	2		1		


	5	4	3	2	1
D					
C					
B					
A					

(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Camera/Touch/DMIC (Reserved</b>			
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	5	4	3	2	1
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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>TPM/Serial (Reserved)</b>			
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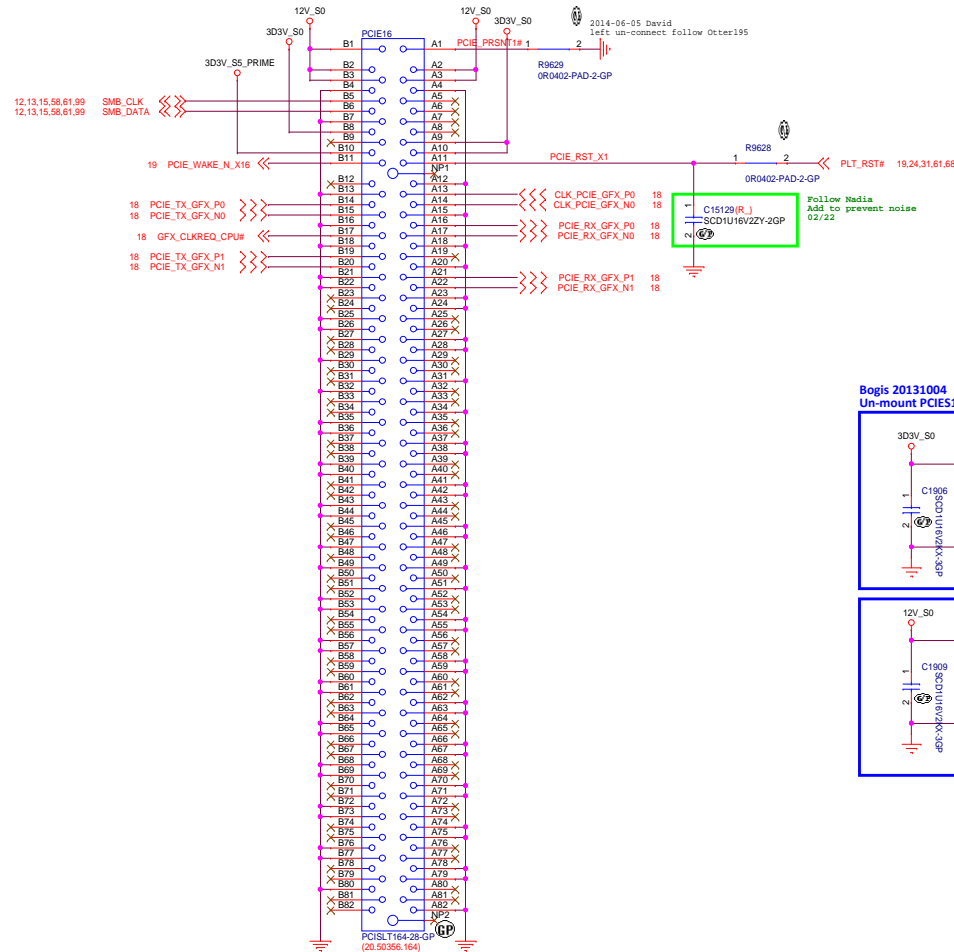
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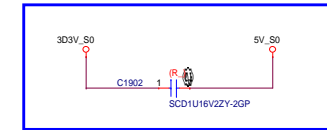
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Title <b>PS2/Parallel</b>			
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PCIEx16 Power Estimation for 75W Card  
 12V\_S0 @ 5.5A  
 3D3V\_S0 @ 3A  
 3D3V\_S5 @ 0.375A

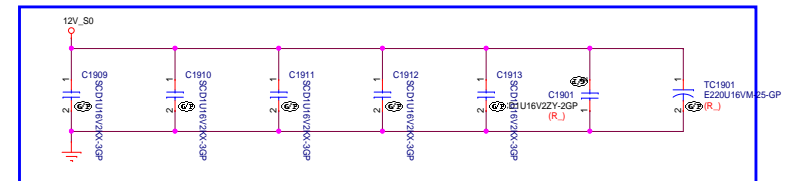
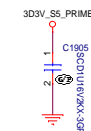
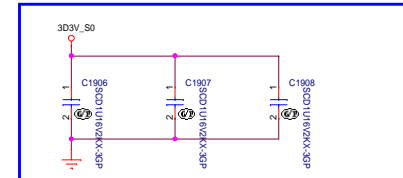
# PCIEx16 CONN



## Cross Moat MLCC




## Bogis 20131004 Un-mount PCIE51 R1903 C1901 C1904-C1913




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B						B
A						A
	5	4	3	2	1	

(Reserved)


		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Smart Card (Reserved)</b>			
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	5	4	3	2	1	
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C						C
B						B
A						A
	5	4	3	2	1	

(Reserved)


		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Scalar (Reserved)</b>			
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		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>MCU (Reserved)</b>			
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		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Intel LAN (Reserved)</b>			
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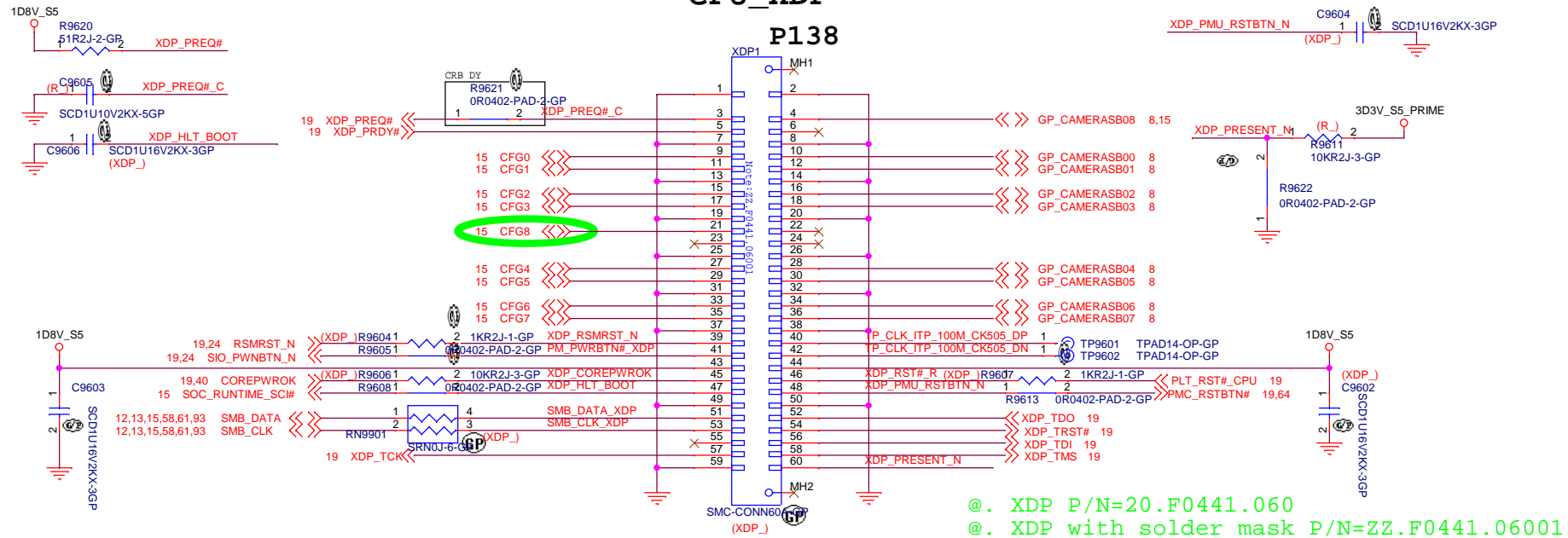
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C						C
B						B
A						A
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(Reserved)

		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>LAN Switch (Reserved)</b>			
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```
SSID = CPU_XDP
```

## CPU\_XDP



Project Name: Brian (4 Layer)  
Project Code: ?  
PCB Number : 14074-SC

On Board Header

CONN	Default	DESCRIPTION
CMOS1	1-2	CMOS CLEAR
ATX1/ATX2		ATX Power 24/20 pin
AUDH1		Audio Front Panel 2x5 pin
FANC1/FANC2		CPU FAN CONN 3/4 pin
XDP1		XDP CONN (CPU Debug)
USB2F1		Front USB 2.0
USB2F2		Front USB 2.0
LEDH1		Front Panel 2x7 pin
DBGH1		Debug Port 2x7
GPIO1		GPIO 1x2 pin
GPIO2		GPIO 1x2 pin
BT1		Battery Holder

XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1501	CPU	19.2M	+/-10ppm CL:7P	C1501=4.7pF C1502=4.7pF
X3502	CPU	32.768K	+/-20ppm CL:7P	C7538=4.7pF C7540=4.7pF
X2101	LAN	25M	+/-20ppm CL:12P	C2116=18pF C2117=18pF
X3501	HUB	12M	+/-30ppm CL:12P	C4603=18pF C4604=18pF
OSC1	SIO	48M		


	ES0(0806)	ES0(1008)	
		ADP	PSU
R			
XDP	V	V	V
HUB	V	V	V
NOHUB			
VGA	V		V
HDMI1		V	
ADP		V	
PSU			V
O		V	
O6		V	
O9			
HUBADP			
HUBPSU			
FUSB3			
DEBUG			

CPU  
pre-SA ES0(0806)  
071.BRASW.000U : 936006 QGQN  
IC CPU INTEL BRASWELL A3 4C 1.36 GHZ GT  
071.00BDW.0F0U : 936011 QGQP  
IC CPU BDW A3 4C NON GT 1.36 GHZ BGA  
  
SA ES0(1008)  
071.BRASW.0A0U : 936006 QGQN  
IC CPU INTEL BRASWELL A3 4C 1.36 GHZ GT  
  
SB ES(1027)  
071.00BDW.0F0U : 936011 QGQP  
IC CPU BDW A3 4C NON GT 1.36 GHZ BGA  
  
SC ES(1126)  
071.BRASL.0A0U : 939009 QHAW  
IC CPU BRASWELL 4C 16EU 1.36GHZ BGA  
071.BRASL.000U : 939018 QHAX  
IC CPU BRASWELL 4C 12EU 1.36GHZ BGA  
  
SC pre-QS(0204 rework at WIH)  
940503 QHMQ  
4C 12EU 2.4GHZ BGA  
940505 QHMS  
4C 16EU 2.24GHZ BGA  
  
1A QS(0305)  
071.00BSW.0B0U :  
071.00BSW.0C0U :  
071.00BSW.0D0U :

-1  
KC.37001.DSP : CPU(BGA) Intel Pentium Quad-Core N3700 2.4G 2M 6W Braswell  
KC.31501.DSC : CPU(BGA) Intel Celeron Quad-Core N3150 2.08G 2M 6W Braswell  
KC.30501.DSC : CPU(BGA) Intel Celeron N3050 2.16G 2M 6W Braswell

BOM Configuration

- R - unmount
- XDP - XDP function
- HUB - USB2.0 hub
- NOHUB - w/o USB2.0 hub
- VGA - VGA function
- HDMI1 - HDMI1 function
- ADP - adapter
- PSU - power supply
- O - OCP
- O6 - 65W adapter OCP
- O9 - 90W adapter OCP
- NOOCP - ADP & No OCP
- HUBADP - ADP & USB2.0 hub
- HUBPSU - PSU & USB2.0 hub
- FUSB3 - Front USB3.0
- DEBUG - debug



Wistron Incorporated  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title  
Table of Content/BOM config

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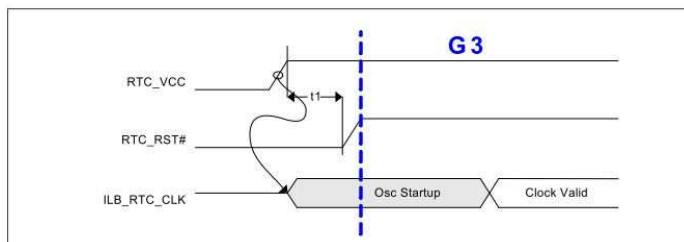
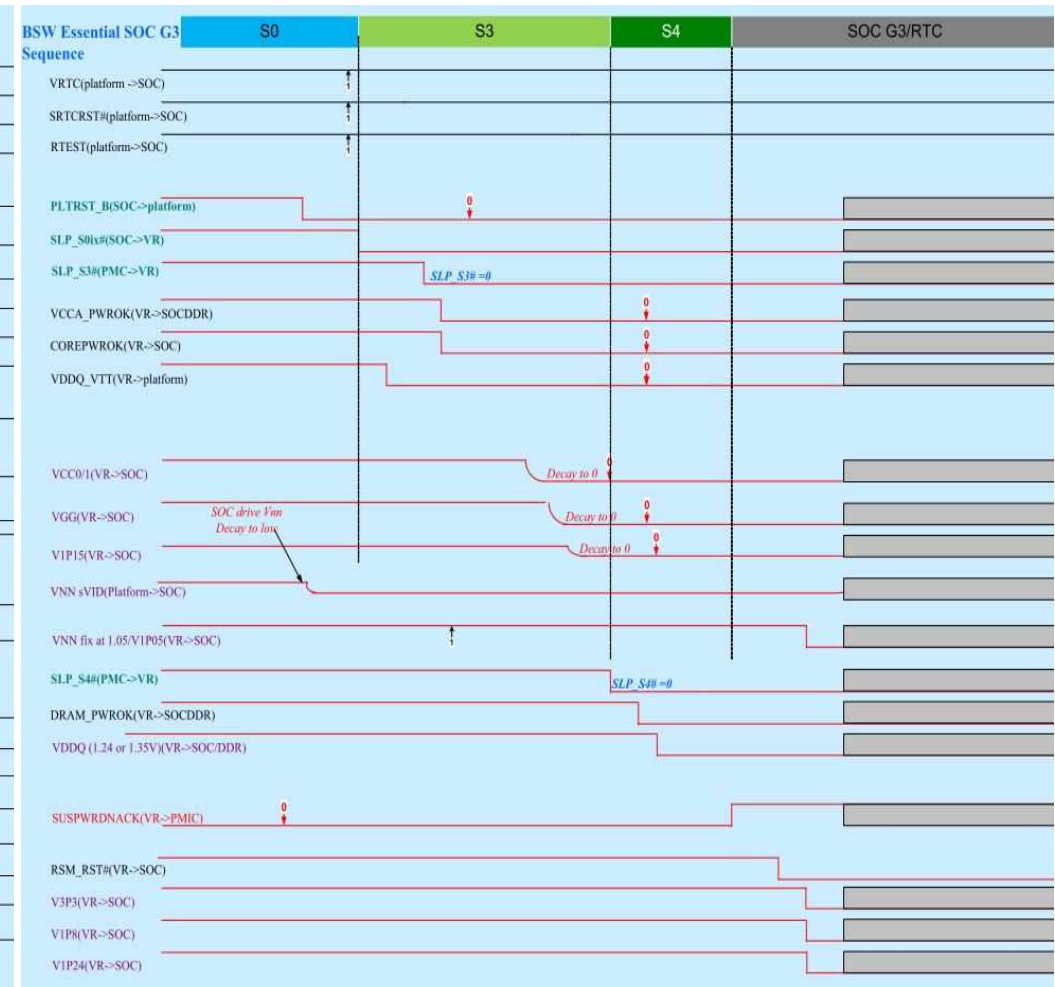
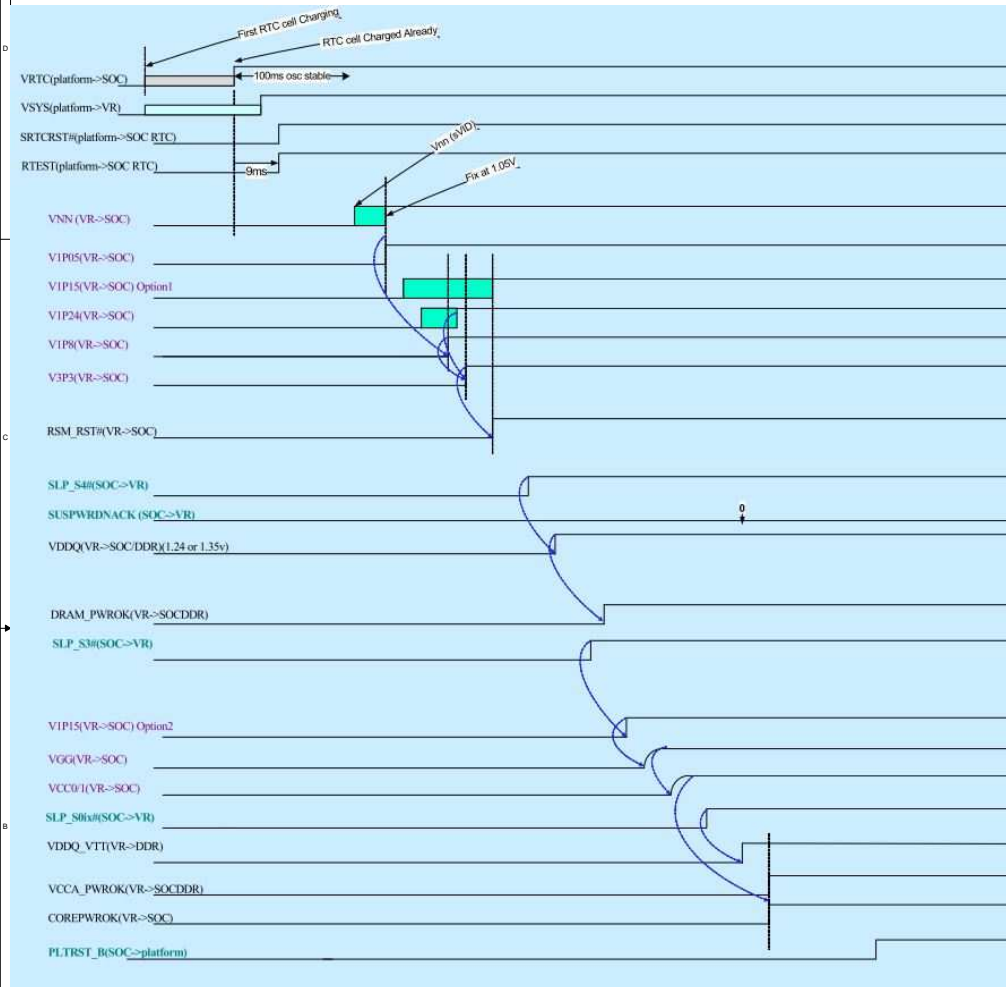
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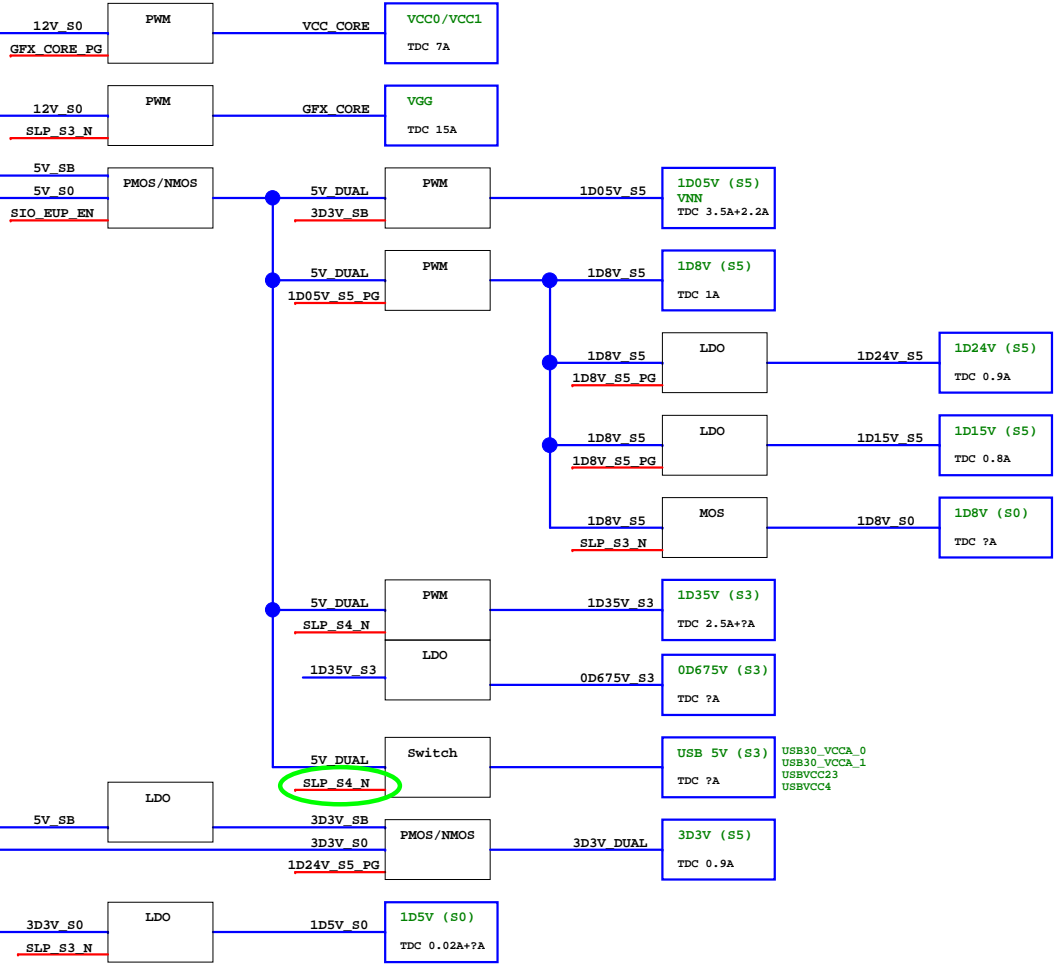
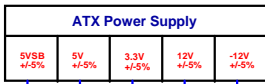
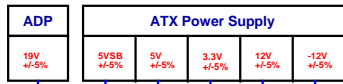
IC Pin Name	Power Well	Default	Default State	Usage	BIOS Programming				
					S0	S1	S3	S4	S5
GENINT1_U/GPIO32	VDD_33	General input	input, 8.2K PU	ID0	GPI	GPI	GPI	GPI	GPI
GENINT2_U/GPIO33	VDD_33	General input	input, 8.2K PU	ID1	GPI	GPI	GPI	GPI	GPI
SCLO/GPIO43	VDD_33	null	input,Tristate	SHB0_CLK	Native	Native	Native	Native	Native
SD_VDD/GPIO45	VDD_33	null	Output HIGH	no use	N/A	N/A	N/A	N/A	N/A
SDA0/GPIO47	VDD_33	null	input, Tri-State	SHB0_DAT_A	Native	Native	Native	Native	Native
SEIRIO/GPIO48	VDD_33	null	input, 8.2K PU	SEIRIO_N	Native	Native	Native	Native	Native
GPIO49	VDD_33	null	input, 8.2K PU	RISER_ID_0	GPI	GPI	GPI	GPI	GPI
	VDD_33	null	input, 8.2K PU	RISER_ID_1	GPI	GPI	GPI	GPI	GPI
GPIO51	VDD_33	null	input, 8.2K PU	PCIE16_DET0	GPI	GPI	GPI	GPI	GPI
FANOUT0/GPIO52	VDD_33	null	input, 8.2K PU	SIO_CLK	GPO	GPO	GPO	GPO	GPO
	VDD_33	null	input, 8.2K PU	SIO_GPO	GPO	GPO	GPO	GPO	GPO
DEVSLP[0]/GPIO55	VDD_33	null	input, 8.2K PU	PCIE16_DET1	GPI	GPI	GPI	GPI	GPI
FANIN0/GPIO56	VDD_33	null	input, 8.2K PU	GPIO	GPO	GPO	GPO	GPO	GPO
GPIO57	VDD_33	null	input, 8.2K PU	XPE_PRESENT	GPO	GPO	GPO	GPO	GPO
GPIO58	VDD_33	null	input, 8.2K PU	PCIE16_DET0	GPI	GPI	GPI	GPI	GPI
DEVSLP[1]/GPIO59	VDD_33	null	input, 8.2K PU	PCIE16_DET1	GPI	GPI	GPI	GPI	GPI
CLK_REQ0_U/									
SATA_1S0_U/					Native	Native	Native	Native	Native
SATA_2P0_U/GPIO60	VDD_33	null	input, 8.2K PU	BLANK_CLK_REQ_N_1					
CLK_REQ1_U/GPIO61	VDD_33	null	input, 8.2K PU	ID0_SLAVE_N	GPO	GPO	GPO	GPO	GPO
CLK_REQ2_U/GPIO62	VDD_33	null	input, 8.2K PU	Test Point	N/A	N/A	N/A	N/A	N/A
CLK_REQ3_U/					GPI	GPI	GPI	GPI	GPI
SATA_1S1_U/					GPO	GPO	GPO	GPO	GPO
SATA_2P1_U/GPIO63	VDD_33	null	input, 8.2K PU	LIM_SEL	GPI	GPI	GPI	GPI	GPI
GPIO64	VDD_33	null	input, 8.2K PU	FP_AUDIO_PRESENCE_N	GPI	GPI	GPI	GPI	GPI
CLK_REQ0_U/GPIO65/					N/A	N/A	N/A	N/A	N/A
OSCIN	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SPKIN/GPIO66	VDD_33	null	input,PU	SPKIN	Native	Native	Native	Native	Native
SATA_ACT_U/GPIO67	VDD_33	null	input, 8.2K PU	FOH_SATA_LED_N	Native	Native	Native	Native	Native
GPIO68	VDD_33	null	input, 8.2K PU	AUD_DET	GPO	GPO	GPO	GPO	GPO
GPIO69	VDD_33	null	input, 8.2K PU	FP_AUDIO_PRESENCE_N	GPI	GPI	GPI	GPI	GPI
GPIO70	VDD_33	null	Tri-State	no use	N/A	N/A	N/A	N/A	N/A
GPIO71	VDD_33	null	Tri-State	APU_PROCHOT#_R	GPO	GPO	GPO	GPO	GPO
SD_CLK/CLK_2/					N/A	N/A	N/A	N/A	N/A
GPIO73	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_CD0/GPIO74	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_CD/GPIO75	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_WP/GPIO76	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA0/					N/A	N/A	N/A	N/A	N/A
SDAT1_2/GPIO77	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA1/					N/A	N/A	N/A	N/A	N/A
SDAT0_2/GPIO78	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA2/GPIO79	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA3/GPIO80	VDD_33	null	input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SPI_WP_U/GPIO161	VDD_33_ALW	null or SPI (strap dependent)	input,PU	no use ROM_RST#	GPO	GPO	GPO	GPO	GPO
SPI_CLK/GPIO162	VDD_33_ALW	null or SPI (strap dependent)	input, 10K PU	SPI_CLK	Native	Native	Native	Native	Native
SPI_DO/GPIO163	VDD_36_ALW	null or SPI (strap dependent)	input, 10K PU	SPI_DATAOUT	Native	Native	Native	Native	Native
SPI_DI/GPIO164	VDD_36_ALW	null or SPI (strap dependent)	input, 10K PU	SPI_DATAIN	Native	Native	Native	Native	Native
SPI_CS1_U/GPIO165	VDD_37_ALW	null or SPI (strap dependent)	input, 10K PU	SPI_CS0#	Native	Native	Native	Native	Native
SPI_CS2_U/GPIO166	VDD_38_ALW	null or SPI (strap dependent)	input, 10K PU	Test Point	N/A	N/A	N/A	N/A	N/A
AZ_S0INO/GPIO167	VDD_38_SVDDIO_AZ_ALW	AZ	input, 50K PU	AZ_S0INO	Native	Native	Native	Native	Native
AZ_S0IN1/GPIO168	VDD_38_SVDDIO_AZ_ALW	AZ	input, 50K PU	AZ_S0IN1	Native	Native	Native	Native	Native
AZ_S0IN2/GPIO169	VDD_38_SVDDIO_AZ_ALW	AZ	input, 50K PU	no use	Native	Native	Native	Native	Native
AZ_S0IN3/GPIO170	VDD_38_SVDDIO_AZ_ALW	AZ	input, 50K PU	no use	Native	Native	Native	Native	Native
GPIO174	VDD_38_ALW	null	input	no use	N/A	N/A	N/A	N/A	N/A
IR_LED_U/L18_U/					N/A	N/A	N/A	N/A	N/A
GPIO184	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
SCLL/GPIO227	VDD_33_ALW	null	input, Tri-State	SM_B1_CLK	Native	Native	Native	Native	Native
SDA1/GPIO228	VDD_33_ALW	null	input, Tri-State	SM_B1_DAT_A	Native	Native	Native	Native	Native
GA20IN/GEVENT0#	VDD_33	null	input, 8.2K PU	KAG20AT_E	Native	Native	Native	Native	Native
GEVENT2#	VDD_33_ALW	null	input, 10K PU	SPI_SW	APU_THERM_TTRIP_N	GPI	GPI	GPI	GPI
LPC_PME#/									
GEVENT3#	VDD_33_ALW	null	input, 10K PU	PMI_ERR_M	Native	Native	Native	Native	Native
GEVENT4#	VDD_33_ALW	null	input, 10K PU	THERM_AL_SHUT#	GPI	GPI	GPI	GPI	GPI
LPC_FDM/									
GEVENT5#	VDD_33_ALW	null	input, 10K PU	LPC_PD_N (Test point)	N/A	N/A	N/A	N/A	N/A
IR_TX1/					N/A	N/A	N/A	N/A	N/A
GEVENT6#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT7#	VDD_33_ALW	DDR3_RST#	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
WAKER/					GPI	GPI	GPI	GPI	GPI
GEVENT8#	VDD_33_ALW	null	input, 10K PU	PC_WAKE_N	Native	Native	Native	Native	Native
SPI_HOLD#/					Native	Native	Native	Native	Native
GEVENT9#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT10#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT11#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
USB_OC0#/									
SPI_TPM_CS#/					Native	Native	Native	Native	Native
TRST#/									
GEVENT12#	VDD_33_ALW	null	input, 10K PU	USB_OC_01	Native	Native	Native	Native	Native
USB_OC1#TDO/									
GEVENT13#	VDD_33_ALW	null	input, 10K PU	USB_OC_02	Native	Native	Native	Native	Native
USB_OC2#TCK/									
GEVENT14#	VDD_33_ALW	null	input, 10K PU	USB_OC_03	Native	Native	Native	Native	Native
USB_OC3#TDO/									
GEVENT15#	VDD_33_ALW	null	input, 10K PU	USB_OC_04	Native	Native	Native	Native	Native

AC_PRES/IR_RXD/	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT15#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT17#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
IR_TXD/	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT21#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
RIM/GEVENT22#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
LPC_SMI#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT23#	VDD_33_ALW	null	input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A

# Braswell Power-up Sequencing

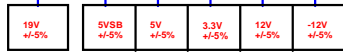
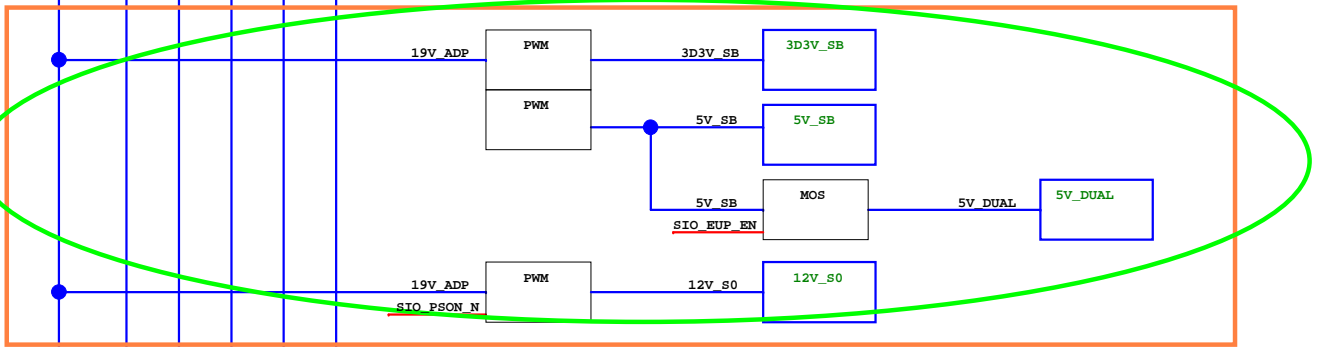
# Braswell Power-Down Sequencing



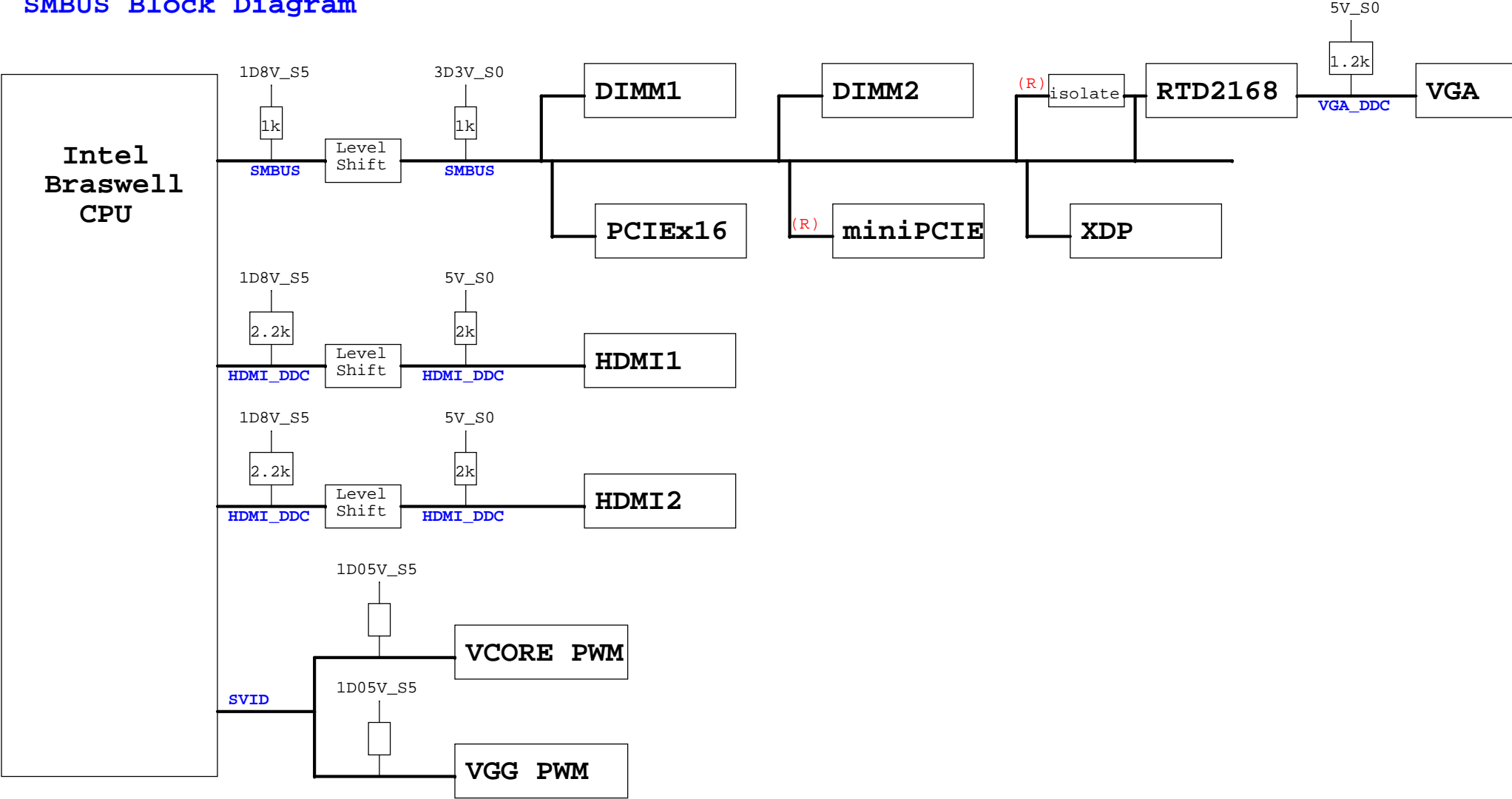


Bay Trail SoC			TDP = 10W
VCCORE	VCCORE	0.700 ~ 1.000V / 15A TDC	
GFX_CORE	GFX_CORE	0.700 ~ 1.000V / 10A TDC	
VIP35S	VIP35S	1.350V / 1.054A	
VIP0A	VIP0A	1.000V / 0.202A	
VIP0S	VIP0S	1.000V / 0.549A	
VIP0SS	VIP0SS	1.050V / 0.720A	
VIP2A	VIP2A	1.200V / 0.035A	
VIP8A	VIP8A	1.800V / 0.051A	
VIP8S	VIP8S	1.800V / 0.002A	
VIP3A	VIP3A	3.300V / 0.002A	
VIP3S	VIP3S	3.300V / 0.002A	
VRVC	VRVC	3.000V / 1.600A	

SO-DIMM			X2
+VDDQ	V_MEM_S	1.350V / 1A	
+DDR3_VTT	V_MEM_VTT	0.875V / 1A	
+3P3V_AUX	PCIE x1	3.3V / 0.5A	
+3P3V_MAIN		3.3V / 0.5A	
+12V_MAIN		12V / 0.5A	
+3P3V_AUX	min-PCI-E (option)	3.3V / 0.5A	
+1P5V_MAIN		1.5V / 0.5A	
+3P3V_AUX	LAN: RTL8111GA	3.3V / 70mA	
+1P5V_MAIN	1.05V/300mA (Internal Switch)		
+3P3V_AUX	SIO: IT872E-EX	3.3V / 300mA	
+3P3V_MAIN		3.3V / 50mA	
+3P3V_AUX	HD CODEC ALC662-VD	3.3V / 300mA	
+3P3V_MAIN		3.3V / 50mA	
VIP8S	BIOS ROM	1.8V / 67mA	
+12V_MAIN	CPU FAN	12V / 200mA	
+12V_MAIN	SYS FAN	12V / 200mA	
USBVCC	USB HUB - GL850-G	5V / 52.4mA	
USBVCC	Charger IC: TPS2544 + USB3.0 VBUS	5V / 2430mA	
USBVCC	USB2.0 VBUS	5V / 500mA	X6
USBVCC	PS/2 KBMS	5V / 275mA	X2
+5V_MAIN	HDD	5V / 858mA	
+12V_MAIN		12V / 662mA	
+5V_MAIN	ODD	5V / 800mA	
+12V_MAIN		12V / 1500mA	

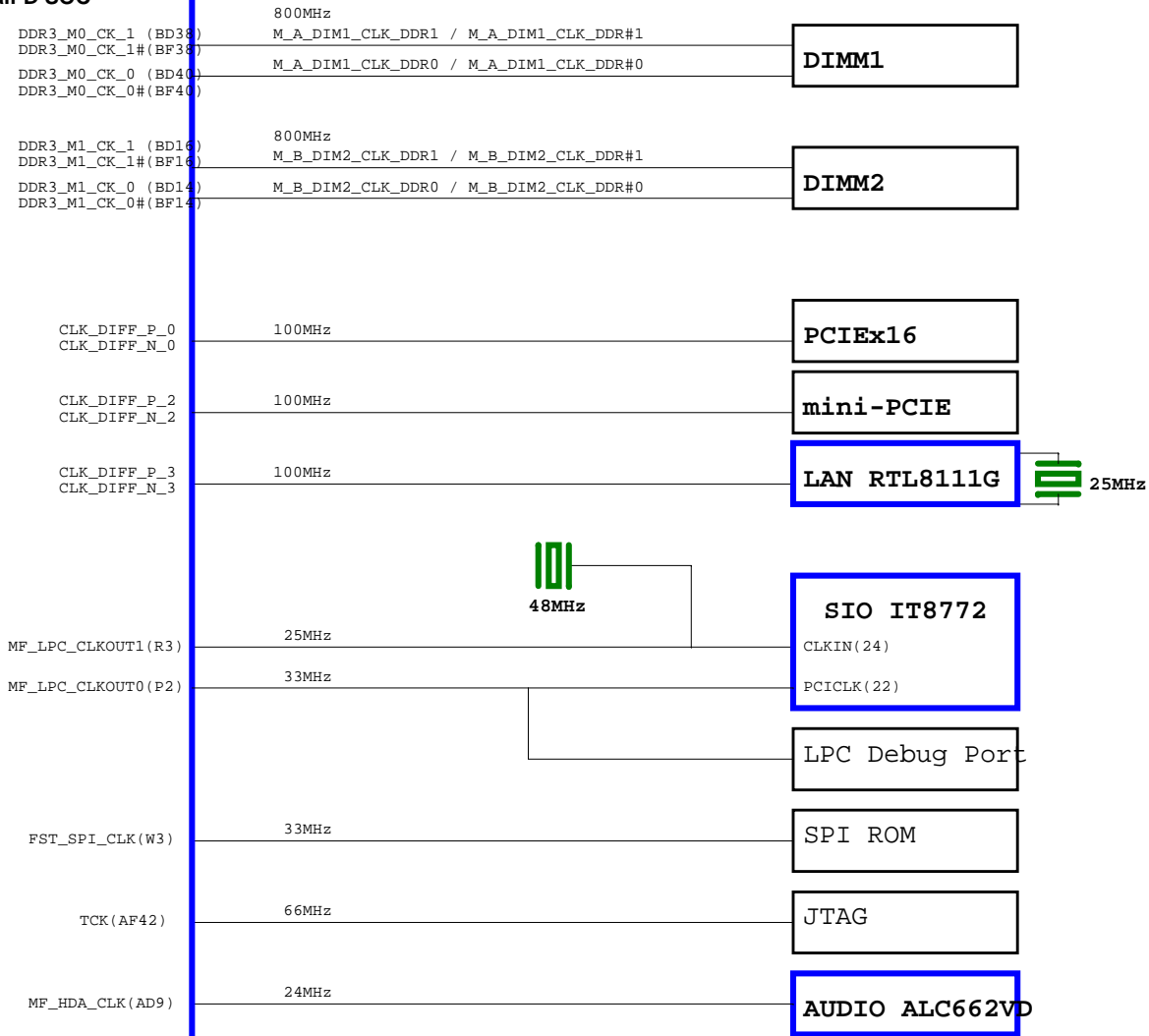


SMBUS Block Diagram

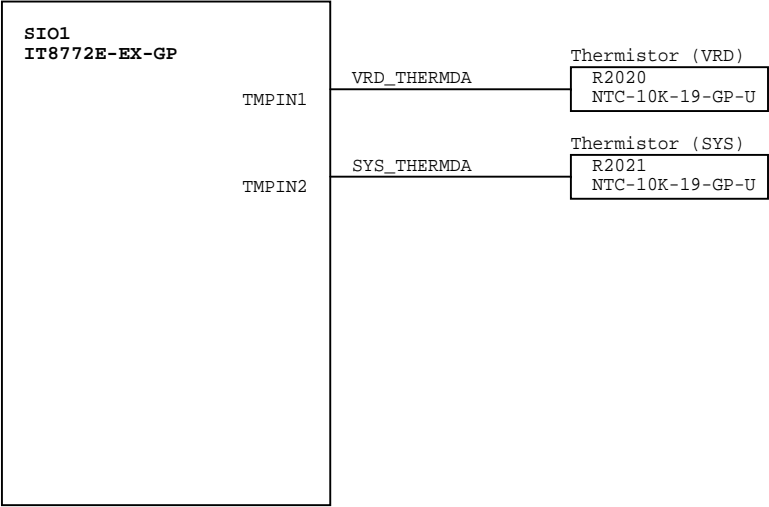
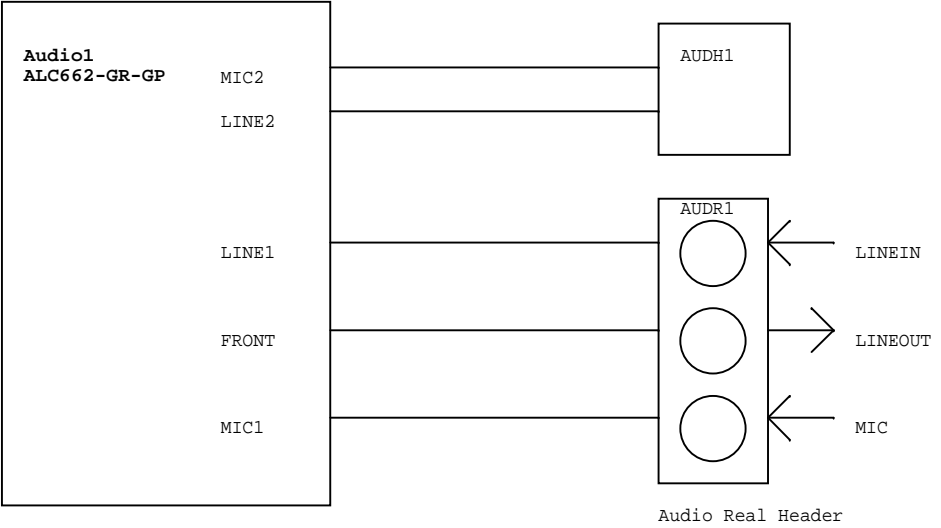


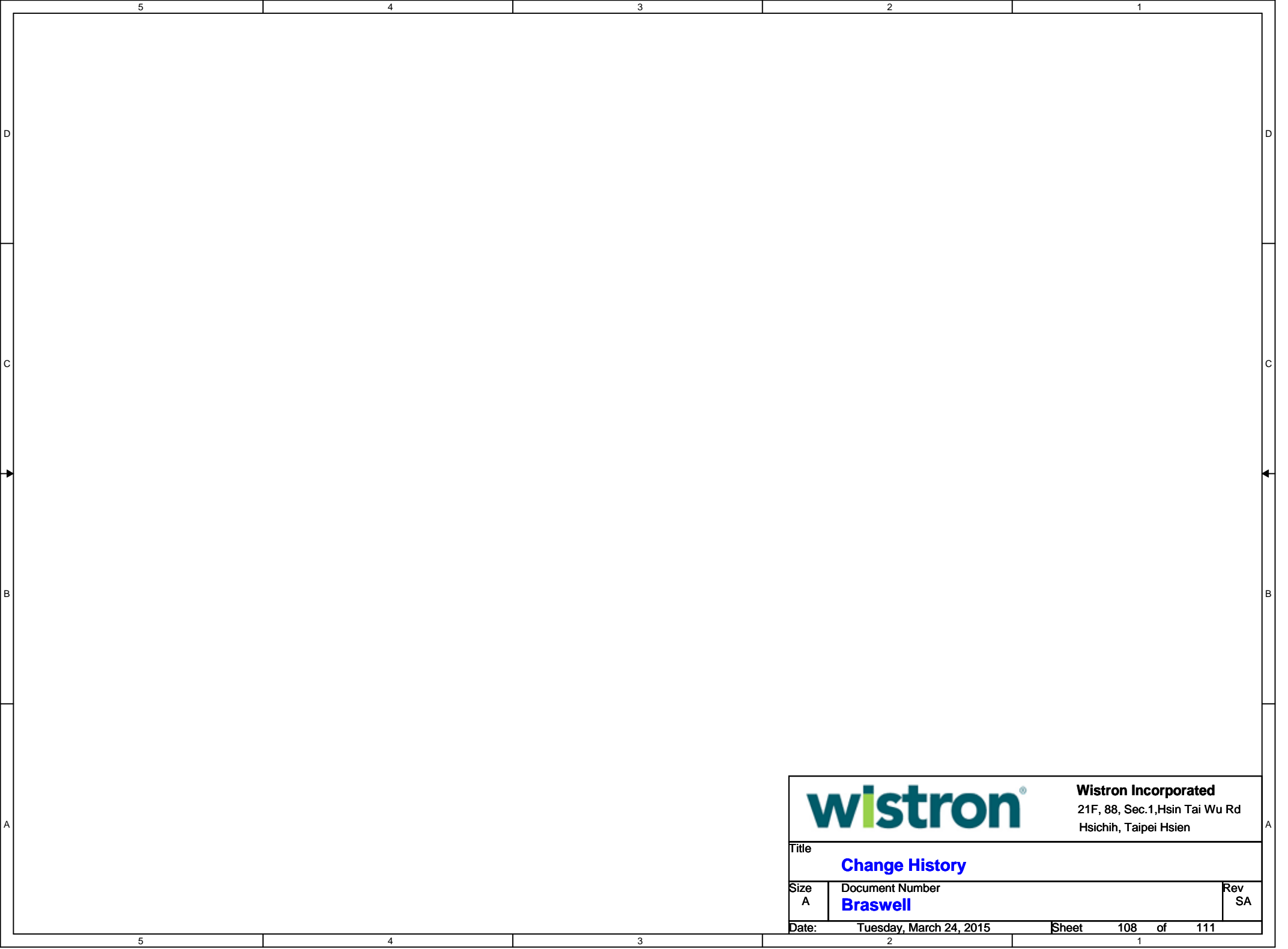



## Bay Trail-D SOC









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